SECTION B: Digital Electronics

Question 1 (15 + 15 = 30 marks)

(a) Reduce the following state table to a minimum number of states.

Present State	Next State X = 0	1	Present Output X = 0	1
a	h	c	1	0
b	c	d	0	1
c	h	b	0	0
d	f	h	0	0
e	c	f	0	1
f	f	g	0	0
g	g	c	1	0
h	a	c	1	0

(b) Implement the circuit described by the reduced state table in part (a) using D flip flops.

Question 2 (10 + 20 = 30 marks)

(a) Write VHDL code for a T flip-flop with an active-high asynchronous clear.

(b) Design the state graph for a Mealy sequential circuit which will produce an output Z=1 for any input sequence X ending in 0011 or 110. The circuit does not reset to the start state when an output of 1 occurs. There is not need to minimise the number of states.

E.g X = 10100110011
Z = 00000011001