# UNIT – 4: Small Signal Analysis of Amplifiers

## 4.1 Basic FET Amplifiers

In the last chapter, we described the operation of the FET, in particular the MOSFET, and analyzed and designed the dc response of circuits containing these devices. In this chapter, we emphasize the use of FETs in linear amplifier applications. Although a major use of MOSFETs is in digital applications, they are also used in linear amplifier circuits.

There are three basic configurations of single-stage or single-transistor FET amplifiers. These are the common-source, source-follower, and common-gate configurations. We investigate the characteristics of each configuration and show how these properties are used in various applications. Since MOSFET integrated circuit amplifiers normally use MOSFETs as load devices instead of resistors because of their small size, we introduce the technique of using MOSFET enhancement or depletion devices as loads. These three configurations form the building blocks for more complex amplifiers, so gaining a good understanding of these three amplifier circuits is an important goal of this chapter.

In integrated circuit systems, amplifiers are usually connected in series or cascade, forming a multistage configuration, to increase the overall voltage gain, or to provide a particular combination of voltage gain and output resistance. We consider a few of the many possible multistage configurations, to introduce the analysis methods required for such circuits, as well as their properties.

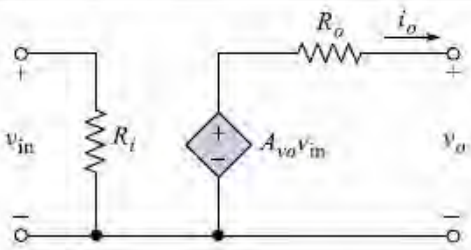
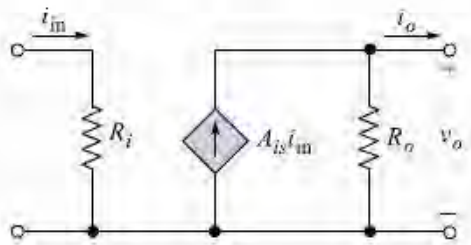
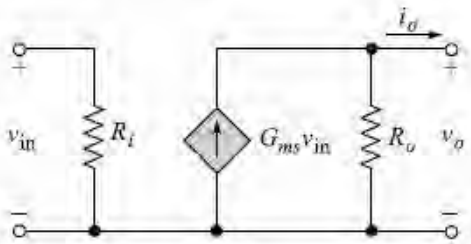
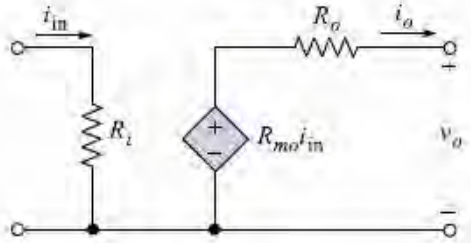
## 4.2 THE MOSFET AMPLIFIER

We discussed the reasons linear amplifiers are necessary in analog electronic systems. In this chapter, we continue the analysis and design of linear amplifiers that use field-effect transistors as the amplifying device. The term small signal means that we can linearize the ac equivalent circuit. We will define what is meant by small signal in the case of MOSFET circuits. The term linear amplifiers means that we can use superposition so that the dc analysis and ac analysis of the circuits can be performed separately and the total response is the sum of the two individual responses.

The mechanism with which MOSFET circuits amplify small time-varying signals was introduced in the last chapter. In this section, we will expand that discussion using the graphical technique, dc load line, and ac load line. In the process, we will develop the various small-signal parameters of linear circuits and the corresponding equivalent circuits.

There are four possible equivalent circuits that can he used.

**Table 4.3** Four equivalent two-port networks

| Type | Equivalent circuit | Gain property |
|---|---|---|
| Voltage amplifier |  | Output voltage proportional to input voltage |
| Current amplifier |  | Output current proportional to input current |
| Transconductance amplifier |  | Output current proportional to input voltage |
| Transresistance amplifier |  | Output voltage proportional to input current |

The most common equivalent circuit that is used for the FET amplifiers is the transconductance amplifier, in which the input signal is a voltage and the output signal is a current.

**Graphical Analysis, Load Lines, and Small-Signal Parameters**

Figure 6. 1 shows an NMOS common-source circuit with a time-varying voltage source in series with the dc source. We assume the time-varying input signal is sinusoidal. Figure 6.2 shows the transistor characteristics, dc load line, and Q-point, where the dc load line and Q-point are functions of $v_{GS}$, $V_{DD}$, $R_D$ and the transistor parameters.

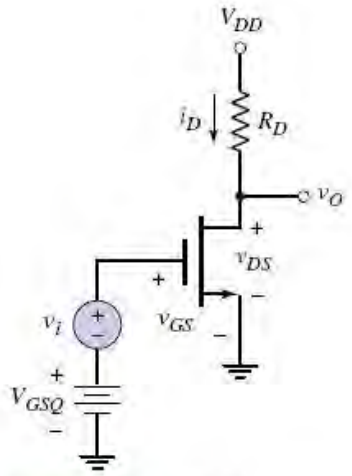



**Figure 6.1** NMOS common-source circuit with time-varying signal source in series with gate dc source

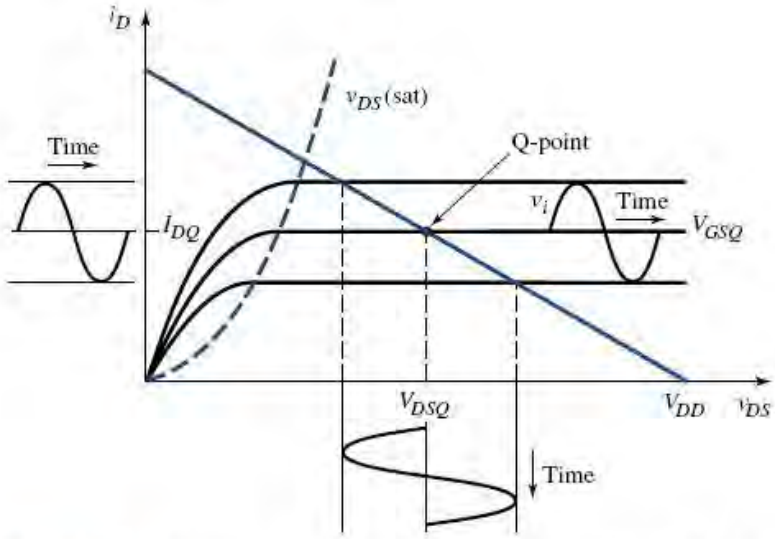



**Figure 6.2** Common-source transistor characteristics, dc load line, and sinusoidal variation in gate-to-source voltage, drain current, and drain-to-source voltage

For the output voltage to be a linear function of the input voltage, the transistor must be biased in the saturation region. Note that, although we primarily use n-channel, enhancement -mode MOSFETs in our discussions, the same results apply to the other MOSFETs.

Also shown in Figure 6.2 are the sinusoidal variations in the gate-to-source voltage, drain current, and drain-to-source voltage, as a result of the sinusoidal source $v_i$. The total gate-to-source voltage is the sum of $V_{GSQ}$ and $v_i$. As $v_i$ increases, the instantaneous value of $v_{GS}$ increases, and the bias point moves up the load line. A larger value of $v_{GS}$ means a larger drain current and a smaller value of $v_{DS}$. Once the Q-point is established, we can develop a mathematical model for the sinusoidal, or small-signal, variations in the gate-to-source voltage, drain-to-source voltage, and drain current.

The time-varying signal source in Figure 6.1 generates a time-varying component of the gate-to-source voltage. For the FET to operate as a linear amplifier, the transistor must be biased in the saturation region, and the instantaneous drain current and drain-to-source voltage must also be confined to the saturation region.

**Transistor Parameters**

The instantaneous gate-to-source voltage is

$$v_{GS} = V_{GSQ} + v_i = V_{GSQ} + v_{gs} \tag{6.1}$$

where $V_{GSQ}$ is the dc component and $v_{gs}$ is the ac component. The instantaneous drain current is

$$i_D = K_n(v_{GS} - V_{TN})^2 \tag{6.2}$$

Substituting Equation (6.1) into (6.2) produces

$$i_D = K_n[V_{GSQ} + v_{gs} - V_{TN}]^2 = K_n[(V_{GSQ} - V_{TN}) + v_{gs}]^2 \tag{6.3(a)}$$

or

$$i_D = K_n(V_{GSQ} - V_{TN})^2 + 2K_n(V_{GSQ} - V_{TN})v_{gs} + K_n v_{gs}^2 \tag{6.3(b)}$$

The first term in Equation (6.3(b)) is the dc or quiescent drain current $I_{DQ}$, the second term is the time-varying drain current component that is linearly related to the signal $v_{gs}$, and the third term is proportional to the square of the signal voltage. For a sinusoidal input signal, the squared term produces undesirable harmonics, or nonlinear distortion, in the output voltage. To minimize these harmonics, we require

$$v_{gs} \ll 2(V_{GSQ} - V_{TN}) \tag{6.4}$$

which means that the third term in Equation (6.3(b)) will be much smaller than the second term. *Equation (6.4) represents the small-signal condition that must be satisfied for linear amplifiers.*

Neglecting the $v_{gs}^2$ term, we can write Equation (6.3(b))

$$i_D = I_{DQ} + i_d \tag{6.5}$$

Again, small-signal implies linearity so that the total current can be separated into a dc component and an ac component. The ac component of the drain current is given by

$$i_d = 2K_n(V_{GSQ} - V_{TN})v_{gs} \tag{6.6}$$

The small-signal drain current is related to the small-signal gate-to-source voltage by the transconductance $g_m$. The relationship is

$$g_m = \frac{i_d}{v_{gs}} = 2K_n(V_{GSQ} - V_{TN}) \tag{6.7}$$

The transconductance is a transfer coefficient relating output current to input voltage and can be thought of as representing the gain of the transistor.

The transconductance can also be obtained from the derivative

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GSQ}=\text{const.}} = 2K_n(V_{GSQ} - V_{TN}) \tag{6.8(a)}$$

which can be written

$$g_m = 2\sqrt{K_n I_{DQ}} \tag{6.8(b)}$$

The drain current versus gate-to-source voltage for the transistor biased in the saturation region is given in Equation (6.2) and is shown in Figure 6.3. The transconductance $g_m$ is the slope of the curve. If the time-varying signal $v_{gs}$ is sufficiently small, the transconductance $g_m$ is a constant. With the $Q$-point in the saturation region, the transistor operates as a current source that is linearly controlled by $v_{gs}$. If the $Q$-point moves into the nonsaturation region, the transistor no longer operates as a linearly controlled current source.

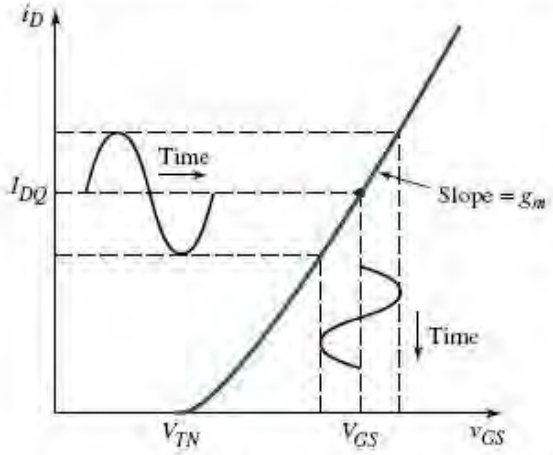



**Figure 6.3** Drain current versus gate-to-source voltage characteristics, with superimposed sinusoidal signals

As shown in Equation (6.8(a)), the transconductance is directly proportional to the conduction parameter $K_n$, which in turn is a function of the width-to-length ratio. Therefore, increasing the width of the transistor increases the transconductance, or gain, of the transistor.

**Comment:** The transconductance of a bipolar transistor is $g_m = (I_{CQ}/V_T)$, which is 38.5 mA/V for a collector current of 1 mA. The transconductance values of MOSFETs tend to be small compared to those of BJTs. However, the advantages of MOSFETs include high input impedance, small size, and low power dissipation.

### AC Equivalent Circuit

From Figure 6.1, we see that the output voltage is

$$v_{DS} = v_O = V_{DD} - i_D R_D \tag{6.9}$$

Using Equation (6.5), we obtain

$$v_O = V_{DD} - (I_{DQ} + i_d)R_D = (V_{DD} - I_{DQ}R_D) - i_d R_D \tag{6.10}$$

The output voltage is also a combination of dc and ac values. The time-varying output signal is the time-varying drain-to-source voltage, or

$$v_o = v_{ds} = -i_d R_D \tag{6.11}$$

Also, from Equations (6.6) and (6.7), we have

$$i_d = g_m v_{gs} \tag{6.12}$$

In summary, the following relationships exist between the time-varying signals for the circuit in Figure 6.1. The equations are given in terms of the instantaneous ac values, as well as the phasors. We have

$$v_{gs} = v_i \tag{6.13(a)}$$

or

$$V_{gs} = V_i \tag{6.13(b)}$$

and

$$i_d = g_m v_{gs} \tag{6.14(a)}$$

or

$$I_d = g_m V_{gs} \tag{6.14(b)}$$

Also,

$$v_{ds} = -i_d R_D \tag{6.15(a)}$$

or

$$V_{ds} = -I_d R_D \tag{6.15(b)}$$

The ac equivalent circuit in Figure 6.4 is developed by setting the dc sources in Figure 6.1 equal to zero. The small-signal relationships are given in Equations (6.13), (6.14), and (6.15). As shown in Figure 6.1, the drain current, which is composed of ac signals superimposed on the quiescent value, flows through the voltage source $V_{DD}$. Since the voltage across this

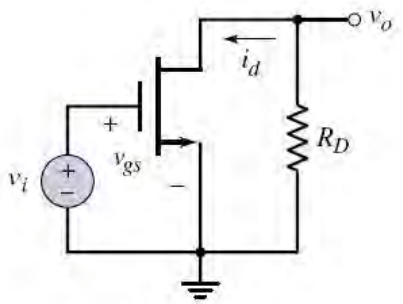



**Figure 6.4** AC equivalent circuit of common-source amplifier with NMOS transistor

source is assumed to be constant, the sinusoidal current produces no sinusoidal voltage component across this element. The equivalent ac impedance is therefore zero, or a short circuit. Consequently, in the ac equivalent circuit, the dc voltage sources are equal to zero. We say that the node connecting $R_D$ and $V_{DD}$ is at signal ground.

## 4.3 Small-Signal Equivalent Circuit

Now that we have the ac equivalent circuit for the NMOS amplifier circuit, (Figure 6.4), we must develop a small-signal equivalent circuit for the transistor.

Initially, we assume that the signal frequency is sufficiently low so that any capacitance at the gate terminal can be neglected. The input to the gate thus appears as an open circuit, or an infinite resistance. Eq. 6.14 relates the small-signal drain current to the small-signal input voltage and Eq. 6.7 shows that the transconductance is a function of the Q-point. The resulting simplified small-signal equivalent circuit for the NMOS device is shown in Figure 6.5. (The phasor components are in parentheses.)

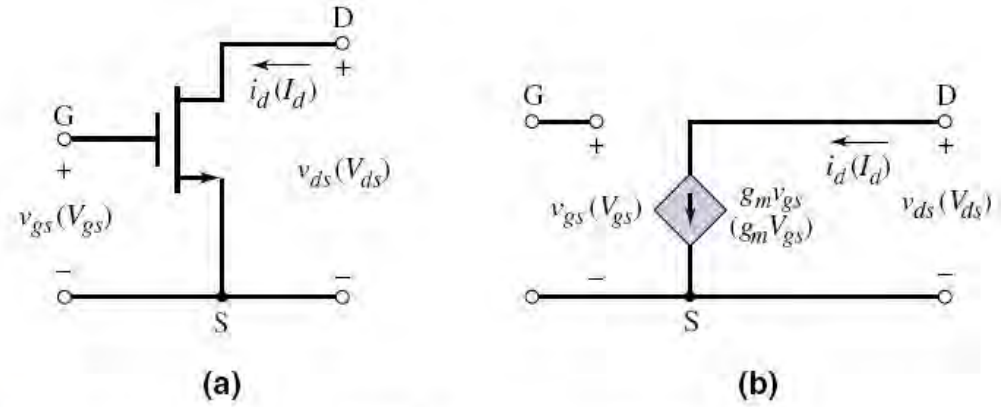



**Figure 6.5** (a) Common-source NMOS transistor with small-signal parameters and (b) simplified small-signal equivalent circuit for NMOS transistor

This small-signal equivalent circuit can also he expanded to take into account the finite output resistance of a MOSFET biased in the saturation region. This effect, discussed in the previous chapter, is a result of the nonzero slope in the $i_D$ versus $v_{DS}$ curve. We know that

$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})] \quad (6.16)$$

where λ is the channel-length modulation parameter and is a positive quantity. The small-signal output resistance, as previously defined, is

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=V_{GSQ}=\text{const.}} \quad (6.17)$$

or

$$r_o = [\lambda K_n(V_{GSQ} - V_{TN})^2]^{-1} \cong [\lambda I_{DQ}]^{-1} \quad (6.18)$$

This small-signal output resistance is also a function of the *Q*-point parameters.

The expanded small-signal equivalent circuit of the n-channel MOSFET is shown in Figure 6.6 in phasor notation.

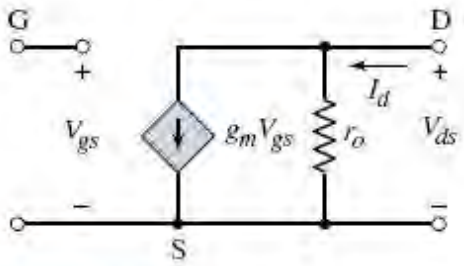



**Figure 6.6** Expanded small-signal equivalent circuit, including output resistance, for NMOS transistor

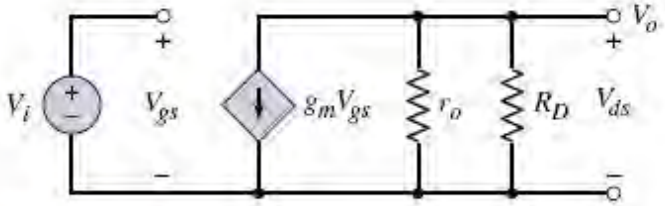



**Figure 6.7** Small-signal equivalent circuit of common-source circuit with NMOS transistor model

We note that the small-signal equivalent circuit for the MOSFET circuit is very similar to that of the BJT circuits.

**Example 6.2** **Objective:** Determine the small-signal voltage gain of a MOSFET circuit.

For the circuit in Figure 6.1, assume parameters are: $V_{GSQ} = 2.12\,\text{V}$, $V_{DD} = 5\,\text{V}$, and $R_D = 2.5\,\text{k}\Omega$. Assume transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n = 0.80\,\text{mA/V}^2$, and $\lambda = 0.02\,\text{V}^{-1}$. Assume the transistor is biased in the saturation region.

**Solution:** The quiescent values are

$$I_{DQ} \cong K_n(V_{GSQ} - V_{TN})^2 = (0.8)(2.12 - 1)^2 = 1.0\,\text{mA}$$

and

$$V_{DSQ} = V_{DD} - I_{DQ}R_D = 5 - (1)(2.5) = 2.5\,\text{V}$$

Therefore,

$$V_{DSQ} = 2.5\,\text{V} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 1.82 - 1 = 0.82\,\text{V}$$

which means that the transistor is biased in the saturation region, as initially assumed, and as required for a linear amplifier. The transconductance is

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(0.8)(2.12 - 1) = 1.79\,\text{mA/V}$$

and the output resistance is

$$r_o = [\lambda I_{DQ}]^{-1} = [(0.02)(1)]^{-1} = 50\,\text{k}\Omega$$

From Figure 6.7, the output voltage is

$$V_o = -g_m V_{gs}(r_o \| R_D)$$

Since $V_{gs} = V_i$, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_d) = -(1.79)(50 \| 2.5) = -4.26$$

Comment: Because of the relatively low value of transconductance, MOSFET circuits tend to have a lower small-signal voltage gain than comparable bipolar circuits. Also, the small-signal voltage gain contains a minus sign, which means that the sinusoidal output voltage is 180 degrees out of phase with respect to the input sinusoidal signal

## 4.4 Problem-Solving Technique: MOSFET AC Analysis

Since we are dealing with linear amplifiers, superposition applies, which means that we can perform the dc and ac analyses separately. The analysis of the MOSFET amplifier proceeds as follows:

1. Analyze the circuit with only the dc sources present. This solution is the dc or quiescent solution. The transistor must he biased in the saturation region in order to produce a linear amplifier.

2. Replace each element in the circuit with its small-signal model, which means replacing the transistor by its small-signal equivalent circuit.

3. Analyze the small-signal equivalent circuit, setting the dc source components equal to zero, to produce the response of the circuit to the time-varying input signals only.

The previous discussion was for an n-channel MOSFET amplifier. The same basic analysts and equivalent circuit also applies to the p-channel transistor. Figure 6.8(a) shows a circuit containing a p-channel MOSFET.

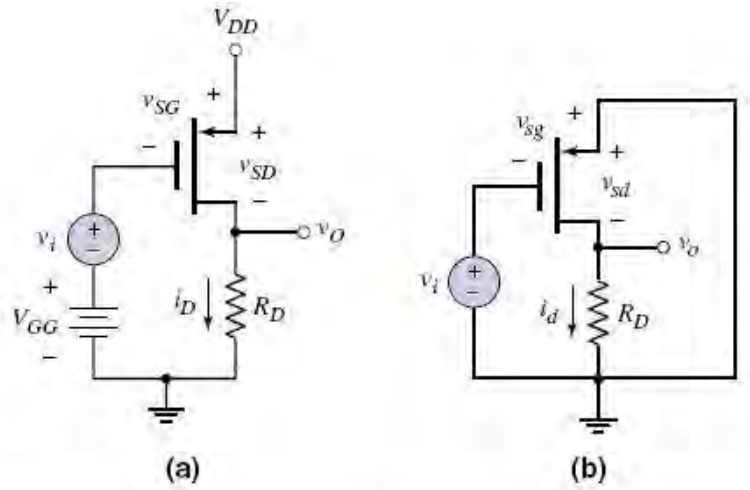



**Figure 6.8** (a) Common-source circuit with PMOS transistor and (b) corresponding ac equivalent circuit

Note that the power supply voltage is connected to the source. (The subscript DD can be used to indicate that the supply is connected to the drain terminal Here, however, $V_{DD}$, is simply the usual notation for the power supply voltage in MOSFET circuits.) Also note the change in current directions and voltage polarities compared to the circuit containing the NMOS transistor. Figure 6.8(b) shows the ac equivalent circuit, with the dc voltage sources replaced

The final small-signal equivalent circuit of the p-channel MOSFET amplifier is shown in Figure 6.10

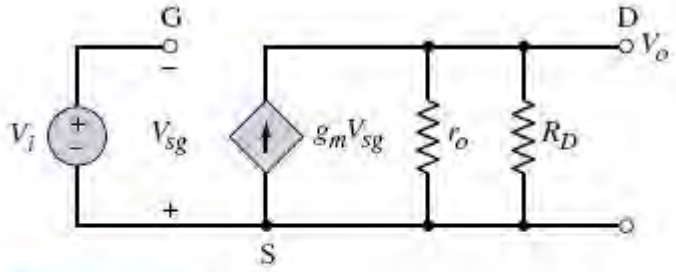



**Figure 6.10** Small-signal equivalent circuit of common-source amplifier with PMOS transistor model

We also note that the expression for the small-signal voltage gain of the p-channel MOSFET amplifier is exactly the same as that for the n-channel MOSFET amplifier. The negative sign indicates that a 180-degree phase reversal exists between the output and input signals, for both the PMOS and the NMOS circuit.

## 4.5 Basic Transistor Amplifier Configurations

As we have seen, the MOSFET is a three-terminal device (actually 4 counting the substrate). Three basic single-transistor amplifier configurations can be formed, depending on which of the three transistor terminals is used as signal ground. These three basic configurations are appropriately called common source, common drain (source follower), and common gate. These three circuit configurations correspond to the common-emitter, emitter-follower, and common-base configurations using BJTs.

The input and output resistance characteristics of amplifiers are important in determining loading effects. These parameters, as well as voltage gain, for the three basic MOSFET circuit configurations will be determined in the following sections.

**THE COMMON-SOURCE AMPLIFIER**

In this section, we consider the first of the three basic circuits; the common-source amplifier. We will analyze several basic common-source circuits, and will determine small-signal voltage gain and input and output impedances.

**A Basic Common-Source Configuration**

For the circuit shown in Figure 6.13, assume that the transistor is biased in the saturation region by resistors $R_1$ and $R_2$, and that the signal frequency is sufficiently large for the coupling capacitor to act essentially as a short circuit. The signal source is represented by a Thevenin equivalent circuit, in which the signal voltage source $v_i$, is in series with an equivalent source resistance $R_{Si}$. As we will see, $R_{Si}$ should be much less than the amplifier input resistance, $R_i = R_1 \parallel R_2$ in order to minimize loading effects.

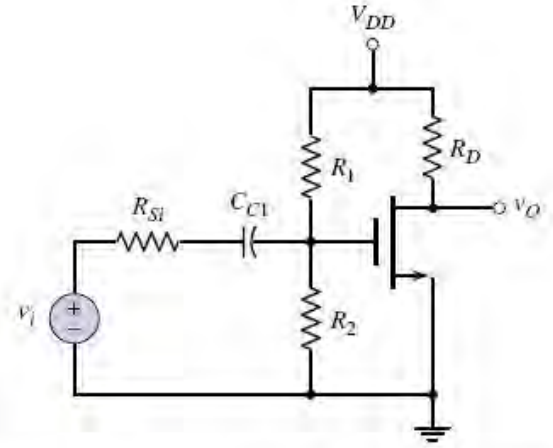



**Figure 6.13** Common-source circuit with voltage divider biasing and coupling capacitor

Figure 6.14 shows the resulting small-signal equivalent circuit. The small signal variables, such as the input signal voltage $V_i$ are given in phasor form.

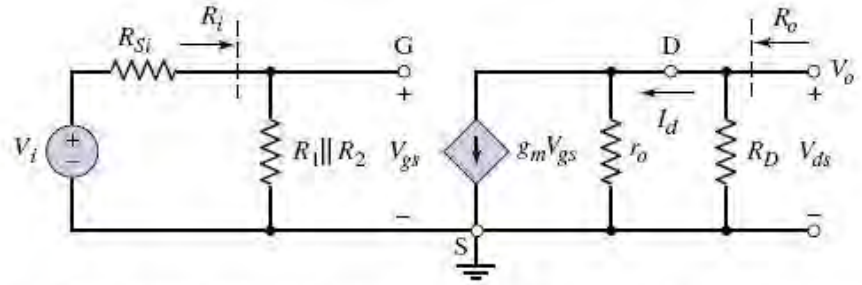



**Figure 6.14** Small-signal equivalent circuit, assuming coupling capacitor acts as a short circuit

The output voltage is

$$V_o = -g_m V_{gs}(r_o \| R_D) \tag{6.27}$$

The input gate-to-source voltage is

$$V_{gs} = \left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i \tag{6.28}$$

so the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_D) \cdot \left(\frac{R_i}{R_i + R_{Si}}\right) \tag{6.29}$$

We can also relate the ac drain current to the ac drain-to-source voltage, as $V_{ds} = -I_d(R_D)$.

Figure 6.15 shows the dc load line, the transition point, and the $Q$-point, which is in the saturation region. As previously stated, in order to provide the maximum symmetrical output voltage swing and keep the transistor biased in the saturation region, the $Q$-point must be near the middle of the saturation region. At the same time, the input signal must be small enough for the amplifier to remain linear.

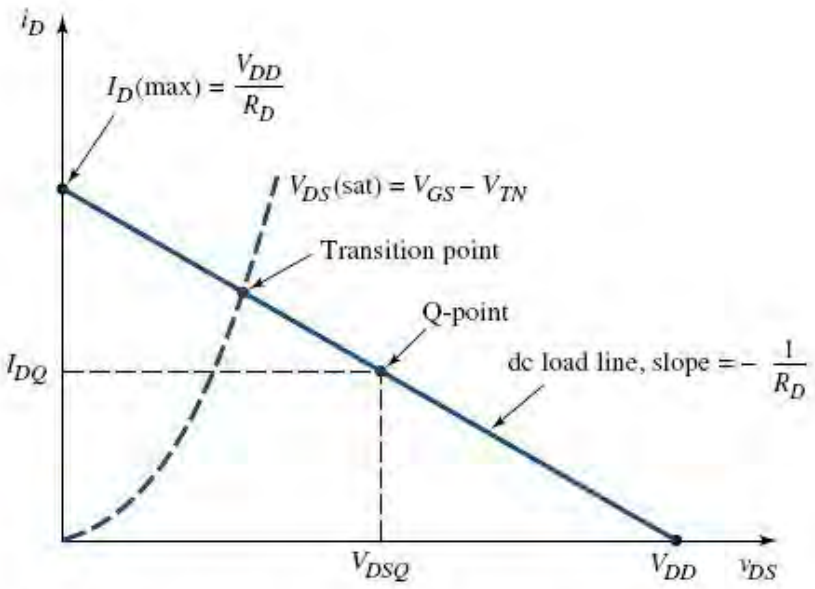



**Figure 6.15** DC load line and transition point separating saturation and nonsaturation regions

The input and output resistances of the amplifier can be determined from Figure 6.14. The input resistance to the amplifier is $R_{is} = R_1 \parallel R_2$. Since the low-frequency input resistance looking into the gate of the MOSFET is essentially infinite, the input resistance is only a function of the bias resistors. The output resistance looking hack into the output terminals is found by setting the independent input source $V_i$ equal to zero, which means that $V_{GS} = 0$. The output resistance is therefore $R_o = R_D \parallel r_o$.

**Example 6.3** **Objective:** Determine the small-signal voltage gain and input and output resistances of a common-source amplifier.

For the circuit shown in Figure 6.13, the parameters are: $V_{DD} = 10\,\text{V}$, $R_1 = 70.9\,\text{k}\Omega$, $R_2 = 29.1\,\text{k}\Omega$, and $R_D = 5\,\text{k}\Omega$. The transistor parameters are: $V_{TN} = 1.5\,\text{V}$, $K_n = 0.5\,\text{mA/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. Assume $R_{Si} = 4\,\text{k}\Omega$.

**Solution:** **DC Calculations**: The dc or quiescent gate-to-source voltage is

$$V_{GSQ} = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{29.1}{70.9 + 29.1}\right)(10) = 2.91\,\text{V}$$

The quiescent drain current is

$$I_{DQ} = K_n(V_{GSQ} - V_{TN})^2 = (0.5)(2.91 - 1.5)^2 = 1\,\text{mA}$$

and the quiescent drain-to-source voltage is

$$V_{DSQ} = V_{DD} - I_{DQ}R_D = 10 - (1)(5) = 5\,\text{V}$$

Since $V_{DSQ} > V_{GSQ} - V_{TN}$, the transistor is biased in the saturation region.

**Small-signal Voltage Gain:** The small-signal transconductance $g_m$ is then

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(0.5)(2.91 - 1.5) = 1.41\,\text{mA/V}$$

and the small-signal output resistance $r_o$ is

$$r_o \cong [\lambda I_{DQ}]^{-1} = [(0.01)(1)]^{-1} = 100\,\text{k}\Omega$$

The amplifier input resistance is

$$R_i = R_1 \| R_2 = 70.9 \| 29.1 = 20.6\,\text{k}\Omega$$

From Figure 6.14 and Equation (6.29), the small-signal voltage gain is

$$A_v = -g_m(r_o \| R_D) \cdot \left(\frac{R_i}{R_i + R_{Si}}\right) = -(1.41)(100 \| 5)\left(\frac{20.6}{20.6 + 4}\right)$$

or

$$A_v = -5.62$$

**Input and Output Resistances:** As already calculated, the amplifier input resistance is

$$R_i = R_1 \| R_2 = 70.9 \| 29.1 = 20.6\,\text{k}\Omega$$

and the amplifier output resistance is

$$R_o = R_D \| r_o = 5 \| 100 = 4.76\,\text{k}\Omega$$

**Comment:** The resulting $Q$-point is in the center of the load line but not in the center of the saturation region. Therefore, this circuit does not achieve the maximum symmetrical output voltage swing in this case.

**Discussion:** The small-signal input gate-to-source voltage is

$$V_{gs} = \left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i = \left(\frac{20.6}{20.6 + 4}\right) \cdot V_i = (0.837) \cdot V_i$$

Since $R_{Si}$ is not zero, the amplifier input signal $V_{gs}$ is approximately 84 percent of the signal voltage. This is again called a loading effect. Even though the input resistance to the gate of the transistor is essentially infinite, the bias resistors greatly influence the amplifier input resistance and loading effect.

**Common-Source Amplifier with Source Resistor**

A source resistor $R_S$ tends to stabilize the Q-point against variations in transistor parameters (Figure 6.18).

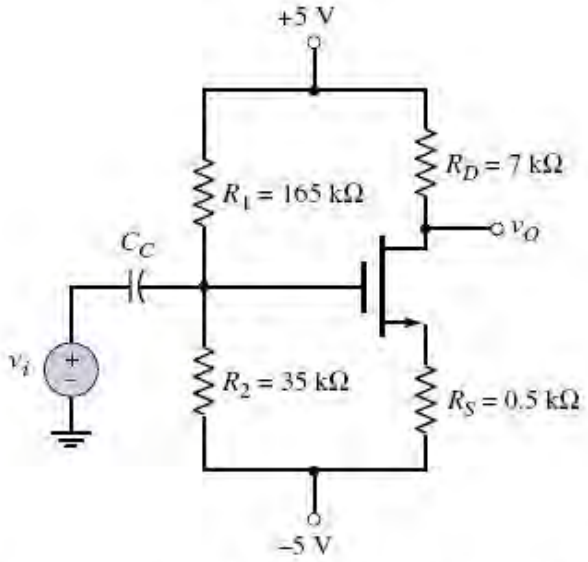



**Figure 6.18** Common-source circuit with source resistor and positive and negative supply voltages

If, for example, the value of the conduction parameter varies from one transistor to another, the Q-point will not vary as much if a source resistor is included in the circuit. However, as shown in the following example, a source resistor also reduces the signal gain. This same effect was observed in BJT circuits when an emitter resistor was included.

The circuit in Figure 6.18 is an example of a situation in which the body effect (not discussed) should be taken into account. The substrate (not shown) would normally be connected to the -5 V supply, so that the body and substrate terminals are not at the same potential. However, in the following example, we will neglect this effect.

**Example 6.5** **Objective:** Determine the small-signal voltage gain of a common-source circuit containing a source resistor.

Consider the circuit in Figure 6.18. The transistor parameters are $V_{TN} = 0.8$ V, $K_n = 1$ mA/V$^2$, and $\lambda = 0$.

**Solution:** From the dc analysis of the circuit, we find that $V_{GSQ} = 1.50\,\text{V}$, $I_{DQ} = 0.50\,\text{mA}$, and $V_{DSQ} = 6.25\,\text{V}$. The small-signal transconductance is

$$g_m = 2K_n(V_{GS} - V_{TN}) = 2(1)(1.50 - 0.8) = 1.4\,\text{mA/V}$$

and the small-signal resistance is

$$r_o \cong [\lambda I_{DQ}]^{-1} = \infty$$

Figure 6.19 shows the resulting small-signal equivalent circuit.

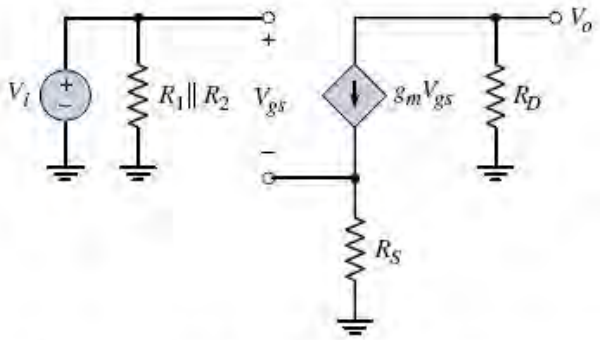



**Figure 6.19** Small-signal equivalent circuit of NMOS common-source amplifier with source resistor

The output voltage is

$$V_o = -g_m V_{gs} R_D$$

Writing a KVL equation from the input around the gate–source loop, we find

$$V_i = V_{gs} + (g_m V_{gs}) R_S = V_{gs}(1 + g_m R_S)$$

or

$$V_{gs} = \frac{V_i}{1 + g_m R_S}$$

The small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_S}$$

We may note that if $g_m$ were large, then the small-signal voltage gain would be approximately

$$A_v \cong \frac{-R_D}{R_S}$$

Substituting the appropriate parameters into the actual voltage gain expression, we find

$$A_v = \frac{-(1.4)(7)}{1 + (1.4)(0.5)} = -5.76$$

**Comment:** A source resistor reduces the small-signal voltage gain. However, as discussed in the last chapter, the $Q$-point is more stabilized against variations in the transistor parameters. We may note that the approximate voltage gain gives $A_v \cong -R_D/R_S = -14$. Since the transconductance of MOSFETs is generally low, the approximate gain expression is a poor one at best.

**Discussion:** We mentioned that including a source resistor tends to stabilize the circuit characteristics against any changes in transistor parameters. If, for example, the conduction parameter $K_n$ varies by ±20 percent, we find the following results.

| $K_n$ (mA/V$^2$) | $g_m$ (mA/V) | $A_v$ |
|---|---|---|
| 0.8 | 1.17 | −5.17 |
| 1.0 | 1.40 | −5.76 |
| 1.2 | 1.62 | −6.27 |

The change in $K_n$ produces a fairly large change in $g_m$. The resulting change in the voltage gain is approximately ±9.5 percent. This change is larger than might be expected because the initial value of $g_m$ is smaller than that of the bipolar circuit.

**Common-Source Circuit with Source Bypass Capacitor**

A source bypass capacitor added to the common-source circuit with a source resistor will minimize the loss in the small-signal voltage gain, while maintaining Q-point stability. The Q-point stability can be further increased by replacing the source resistor with a constant-current source. The resulting circuit is shown in Figure 6.22, assuming an ideal signal source. If the signal frequency is sufficiently large so that the bypass capacitor acts essentially as an ac short-circuit, the source will be held at signal ground.

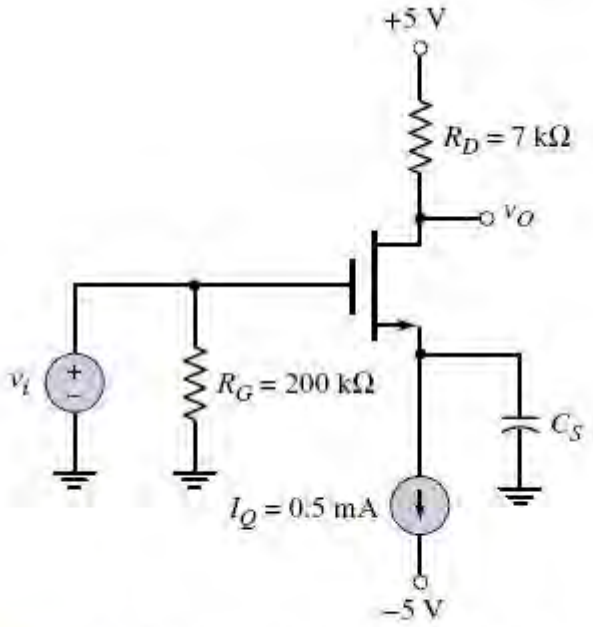



**Figure 6.22** NMOS common-source circuit with source bypass capacitor

**Example 6.6** **Objective:** Determine the small-signal voltage gain of a circuit biased with a constant-current source and incorporating a source bypass capacitor.

For the circuit shown in Figure 6.22, the transistor parameters are: $V_{TN} = 0.8$ V, $K_n = 1$ mA/V$^2$, and $\lambda = 0$.

**Solution:** Since the dc gate current is zero, the dc voltage at the source terminal is $V_S = -V_{GSQ}$, and the gate-to-source voltage is determined from

$$I_{DQ} = I_Q = K_n(V_{GSQ} - V_{TN})^2$$

or

$$0.5 = (1)(V_{GSQ} - 0.8)^2$$

which yields

$$V_{GSQ} = -V_S = 1.51 \text{ V}$$

The quiescent drain-to-source voltage is

$$V_{DSQ} = V_{DD} - I_{DQ}R_D - V_S = 5 - (0.5)(7) - (-1.51) = 3.01 \text{ V}$$

The transistor is therefore biased in the saturation region.

The small-signal equivalent circuit is shown in Figure 6.23. The output voltage is

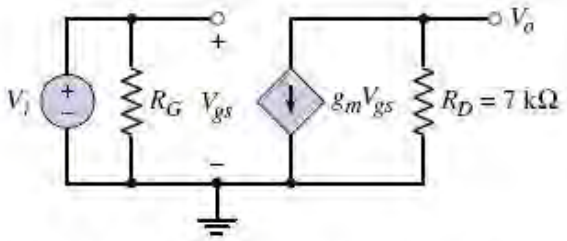



**Figure 6.23** Small-signal equivalent circuit, assuming the source bypass capacitor acts as a short circuit

$$V_o = -g_m V_{gs} R_D$$

Since $V_{gs} = V_i$, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m R_D = -(1.4)(7) = -9.8$$

**Comment:** Comparing the small-signal voltage gain of 9.8 in this example to the 5.76 calculated in Example 6.5, we see that the magnitude of the gain increases when a source bypass capacitor is included.

## 4.6 The Source-Follower Amplifer

The second type of MOSFE'T amplifier to be considered is the common-drain circuit. An example of this circuit configuration is shown in Figure 6.28.

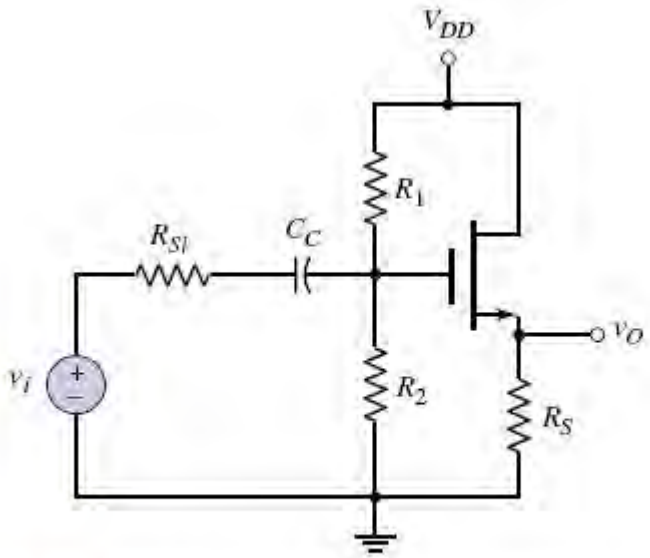



**Figure 6.28** NMOS source-follower or common-drain amplifier

As seen in this figure, the output signal is taken off the source with respect to ground and the drain is connected directly to $V_{DD}$. Since $V_{DD}$ becomes signal ground in the ac equivalent circuit, we get the name common drain, but the more common name is a source follower. The reason for this name will become apparent as we proceed through the analysis.

**Small-Signal Voltage Gain**

The dc analysis of the circuit is exactly the same as we have already seen, so we will concentrate on the small-signal analysis. The small-signal equivalent circuit, assuming the coupling capacitor acts as a short circuit, is shown in Figure 6.29(a). The drain is at signal ground, and the small-signal resistance $r_o$ of the transistor is in parallel with the dependent current source. Figure 6.29(b) is the same equivalent circuit, but with all signal grounds at a common point. We are again neglecting the body effect. The output voltage is

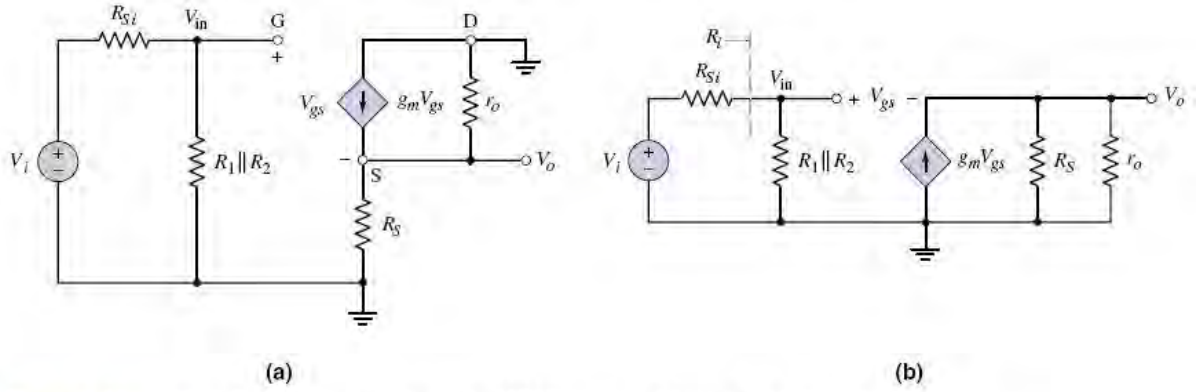



**Figure 6.29** (a) Small-signal equivalent circuit of NMOS source follower and (b) small-signal equivalent circuit of NMOS source follower with all signal grounds at a common point

$$V_o = (g_m V_{gs})(R_s \| r_o) \tag{6.30}$$

Writing a KVL equation from input to output results in the following:

$$V_{\text{in}} = V_{gs} + V_o = V_{gs} + g_m V_{gs}(R_S \| r_o) \tag{6.31(a)}$$

Therefore, the gate-to-source voltage is

$$V_{gs} = \frac{V_{\text{in}}}{1 + g_m(R_S \| r_o)} = \left[\frac{\frac{1}{g_m}}{\frac{1}{g_m} + (R_S \| r_o)}\right] \cdot V_{\text{in}} \tag{6.31(b)}$$

Equation (6.31(b)) is written in the form of a voltage-divider equation, in which the gate-to-source of the NMOS device looks like a resistance with a value of $1/g_m$. More accurately, the effective resistance looking into the source terminal (ignoring $r_o$) is $1/g_m$. The voltage $V_{\text{in}}$ is related to the source input voltage $V_i$ by

$$V_{\text{in}} = \left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i \tag{6.32}$$

where $R_i = R_1 \| R_2$ is the input resistance to the amplifier.

Substituting Equations (6.31(b)) and (6.32) into (6.30), we have the small-signal voltage gain:

$$A_v = \frac{V_o}{V_i} = \frac{g_m(R_S \| r_o)}{1 + g_m(R_S \| r_o)} \cdot \left(\frac{R_i}{R_i + R_{Si}}\right) \tag{6.33(a)}$$

or

$$A_v = \frac{R_S \| r_o}{\frac{1}{g_m} + R_S \| r_o} \cdot \left(\frac{R_i}{R_i + R_{Si}}\right) \tag{6.33(b)}$$

which again is written in the form of a voltage-divider equation. An inspection of Equation 6.33(b) shows that the magnitude of the voltage gain is always less than unity. This result is consistent with the results of the BJT emitter-follower circuit.

**Example 6.7** **Objective:** Calculate the small-signal voltage gain of the source-follower circuit in Figure 6.28.

Assume the circuit parameters are $V_{DD} = 12\,\text{V}$, $R_1 = 162\,\text{k}\Omega$, $R_2 = 463\,\text{k}\Omega$, and $R_S = 0.75\,\text{k}\Omega$, and the transistor parameters are $V_{TN} = 1.5\,\text{V}$, $K_n = 4\,\text{mA/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. Also assume $R_{Si} = 4\,\text{k}\Omega$.

**Solution:** The dc analysis results are $I_{DQ} = 7.97\,\text{mA}$ and $V_{GSQ} = 2.91\,\text{V}$. The small-signal transconductance is therefore

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(4)(2.91 - 1.5) = 11.3\,\text{mA/V}$$

and the small-signal transistor resistance is

$$r_o \cong [\lambda I_{DQ}]^{-1} = [(0.01)(7.97)]^{-1} = 12.5\,\text{k}\Omega$$

The amplifier input resistance is

$$R_i = R_1 \| R_2 = 162 \| 463 = 120\,\text{k}\Omega$$

The small-signal voltage gain then becomes

$$A_v = \frac{g_m(R_S \| r_o)}{1 + g_m(R_S \| r_o)} \cdot \frac{R_i}{R_i + R_{Si}} = \frac{(11.3)(0.75 \| 12.5)}{1 + (11.3)(0.75 \| 12.5)} \cdot \frac{120}{120 + 4} = +0.860$$

**Comment:** The magnitude of the small-signal voltage gain is less than 1. An examination of Equation (6.33(b)) shows that this is always true. Also, the voltage gain is positive, which means that the output signal voltage is in phase with the input signal voltage. Since the output signal is essentially equal to the input signal, the circuit is called a source follower.

**Discussion:** The expression for the voltage gain of the source follower is essentially identical to that of the bipolar emitter follower. Since the transconductance of the BJT is, in general, larger than that of the MOSFET, the voltage gain of the emitter follower will be closer to unity than that of the MOSFET source follower.

Although the voltage gain is slightly less than 1, the source follower is an extremely useful circuit because the output resistance is less than that of a common-source circuit. A small output resistance is desirable when the circuit is to act as an ideal voltage source and drive a load circuit without suffering any loading effects.

## 4.7 Input and Output impedance

The input resistance $R_i$, as defined in Figure 6.29{b), is the Thevenin equivalent resistance of the bias resistors. Even though the input resistance to the gate of the MOSFET is essentially infinite, the input bias resistances do create a loading effect. This same effect was seen in the common-source circuits.

To calculate the output resistance, we set all independent small-signal sources equal to zero, apply a test voltage to the output terminals, and measure a test current. Figure 6.31 shows the circuit we will use to determine the output resistance of the source follower shown in Figure 6.28.

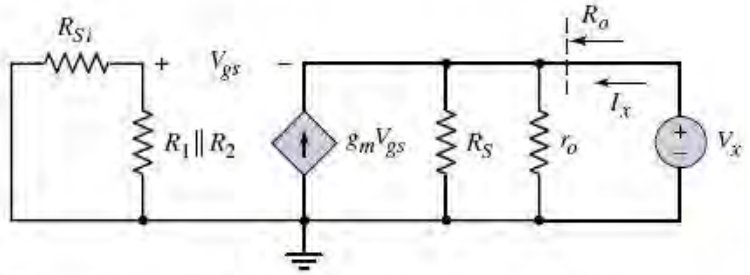



**Figure 6.31** Equivalent circuit of NMOS source follower, for determining output resistance

We set $V_i = 0$ and apply a test voltage $V_x$. Since there are no capacitances in the circuit, the output impedance is simply an output resistance, which is defined as

$R_o = V_x / I_x$

Writing a KCL equation at the output source terminal produces

$$I_x + g_m V_{gs} = \frac{V_x}{R_S} + \frac{V_x}{r_o} \tag{6.35}$$

Since there is no current in the input portion of the circuit, we see that $V_{gs} = -V_x$. Therefore, Equation (6.35) becomes

$$I_x = V_x\left(g_m + \frac{1}{R_S} + \frac{1}{r_o}\right) \tag{6.36(a)}$$

or

$$\frac{I_x}{V_x} = \frac{1}{R_o} = g_m + \frac{1}{R_S} + \frac{1}{r_o} \tag{6.36(b)}$$

The output resistance is then

$$R_o = \frac{1}{g_m} \| R_S \| r_o \tag{6.37}$$

From Figure 6.31, we see that the voltage $V_{gs}$ is directly across the current source $g_m V_{gs}$. This means that the effective resistance of the device is $1/g_m$. The output resistance given by Equation (6.37) can therefore be written directly. This result also means that the resistance looking into the source terminal (ignoring $r_o$) is $1/g_m$, as previously noted.

**Example 6.9** **Objective:** Calculate the output resistance of a source-follower circuit.

Consider the circuit shown in Figure 6.28 with circuit and transistor parameters given in Example 6.7.

**Solution:** The results of Example 6.7 are: $R_S = 0.75\,\text{k}\Omega$, $r_o = 12.5\,\text{k}\Omega$, and $g_m = 11.3\,\text{mA/V}$. Using Figure 6.31 and Equation (6.37), we find

$$R_o = \frac{1}{g_m} \| R_S \| r_o = \frac{1}{11.3} \| 0.75 \| 12.5$$

or

$$R_o = 0.0787\,\text{k}\Omega = 78.7\,\Omega$$

**Comment:** The output resistance of a source-follower circuit is dominated by the transconductance parameter. Also, because the output resistance is very low, the source follower tends to act like an ideal voltage source, which means that the output can drive another circuit without significant loading effects.

## 4.8 The Common-Gate Configuration

The third amplifier configuration is the common-gate circuit. To determine the small-signal voltage and current gains, and the input and output impedances, we will use the same small-signal equivalent circuit for the transistor that was used previously. The dc analysis of the common-gate circuit is the same as that of previous MOSFET circuits.

**Small-Signal Voltage and Current Gains**

In the common-gate configuration, the input signal is applied to the source terminal and the gate is at signal ground. The common-gate configuration shown in Figure 6.344 is biased with a constant-current source $I_Q$.

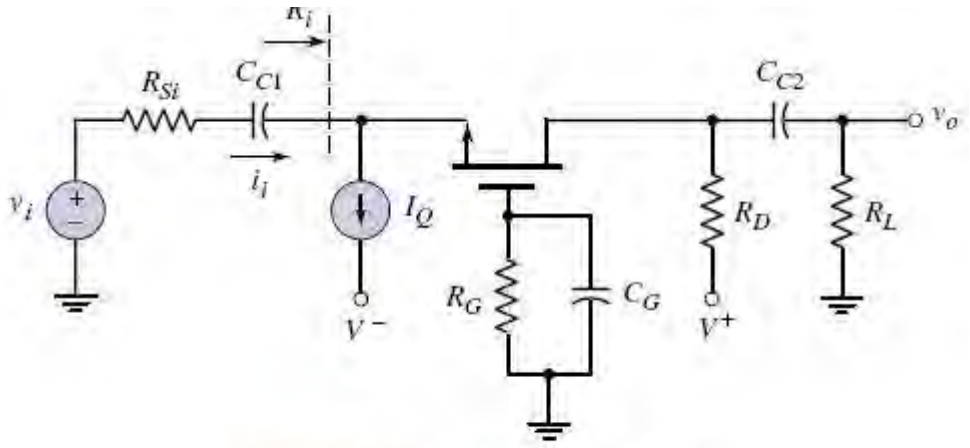



**Figure 6.34** Common-gate circuit

The gate resistor $R_G$ prevents the buildup of static charge on the gate terminal, and the capacitor $C_G$ ensures that the gate is at signal ground. The coupling capacitor $C_{C1}$ couples the signal to the source, and coupling capacitor $C_{C2}$ couples the output voltage to load resistance $R_L$.

The small-signal equivalent circuit is shown in Figure 6.35. The small-signal transistor resistance $r_O$ is assumed to be infinite.

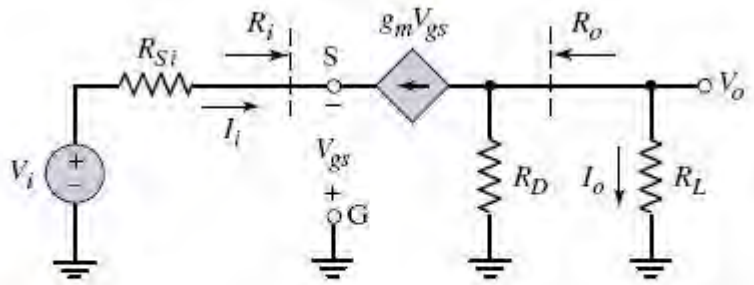



**Figure 6.35** Small-signal equivalent circuit of common-gate amplifier

The output voltage is

$$V_o = -(g_m V_{gs})(R_D \| R_L) \tag{6.38}$$

Writing the KVL equation around the input, we find

$$V_i = I_i R_{Si} - V_{gs} \tag{6.39}$$

where $I_i = -g_m V_{gs}$. The gate-to-source voltage can then be written as

$$V_{gs} = \frac{-V_i}{1 + g_m R_{Si}} \tag{6.40}$$

The small-signal voltage gain is found to be

$$A_v = \frac{V_o}{V_i} = \frac{g_m(R_D \| R_L)}{1 + g_m R_{Si}} \tag{6.41}$$

Also, since the voltage gain is positive, the output and input signals are in phase.

In many cases, the signal input to a common-gate circuit is a current. Figure 6.36 shows the small-signal equivalent common-gate circuit with a Norton equivalent circuit as the signal source. We can calculate a current gain. The output current $I_o$ can be written

$$I_o = \left(\frac{R_D}{R_D + R_L}\right)(-g_m V_{gs}) \tag{6.42}$$

At the input we have

$$I_i + g_m V_{gs} + \frac{V_{gs}}{R_{Si}} = 0 \tag{6.43}$$

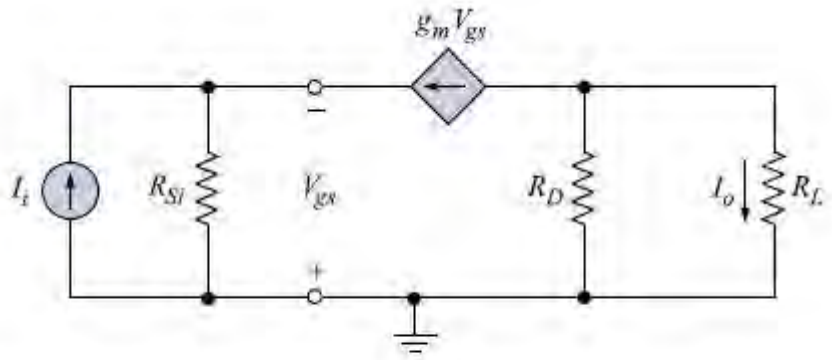



**Figure 6.36** Small-signal equivalent circuit of common-gate amplifier with a Norton equivalent signal source

or

$$V_{gs} = -I_i\left(\frac{R_{Si}}{1 + g_m R_{Si}}\right) \tag{6.44}$$

The small-signal current gain is then

$$A_i = \frac{I_o}{I_i} = \left(\frac{R_D}{R_D + R_L}\right) \cdot \left(\frac{g_m R_{Si}}{1 + g_m R_{Si}}\right) \tag{6.45}$$

We may note that if $R_D \gg R_L$ and $g_m R_{Si} \gg 1$, then the current gain is essentially unity as it is for an ideal BJT common-base circuit.

**Input and Output Impedance**

In contrast to the common-source and source-follower amplifiers, the common-gate circuit has a low input resistance because of the transistor. However, if the input signal is a current, a low input resistance is an advantage. The input resistance is defined as

$$R_i = \frac{-V_{gs}}{I_i} \tag{6.46}$$

Since $I_i = -g_m V_{gs}$, the input resistance is

$$R_i = \frac{1}{g_m} \tag{6.47}$$

This result has been obtained previously.

We can find the output resistance by setting the input signal voltage equal to zero. From Figure 6.35, we see that $V_{gs} = -g_m V_{gs} R_{Si}$, which means that $V_{gs} = 0$. Consequently, $g_m V_{gs} = 0$. The output resistance, looking back from the load resistance, is therefore

$$R_o = R_D \tag{6.48}$$

**Example 6.10** **Objective:** For the common-gate circuit, determine the output voltage for a given input current.

For the circuits shown in Figures 6.34 and 6.36, the circuit parameters are: $I_Q = 1\,\text{mA}$, $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_G = 100\,\text{k}\Omega$, $R_D = 4\,\text{k}\Omega$, and $R_L = 10\,\text{k}\Omega$. The transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0$. Assume the input current is $100 \sin \omega t\,\mu\text{A}$ and assume $R_{Si} = 50\,\text{k}\Omega$.

**Solution:** The quiescent gate-to-source voltage is determined from

$$I_Q = I_{DQ} = K_n(V_{GSQ} - V_{TN})^2$$

or

$$1 = 1(V_{GSQ} - 1)^2$$

which yields

$$V_{GSQ} = 2\,\text{V}$$

The small-signal transconductance is

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(1)(2-1) = 2\,\text{mA/V}$$

From Equation (6.45), we can write the output current as

$$I_o = I_i\left(\frac{R_D}{R_D + R_L}\right)\cdot\left(\frac{g_m R_{Si}}{1 + g_m R_{Si}}\right)$$

The output voltage is $V_o = I_o R_L$, so we find

$$V_o = I_i\left(\frac{R_L R_D}{R_D + R_L}\right)\cdot\left(\frac{g_m R_{Si}}{1 + g_m R_{Si}}\right)$$

$$= \left[\frac{(10)(4)}{4+10}\right]\cdot\left[\frac{(2)(50)}{1+(2)(50)}\right]\cdot(0.1)\sin\omega t$$

or

$$V_o = 0.283\sin\omega t\,\text{V}$$

**Comment:** As with the BJT common-base circuit, the MOSFET common-gate amplifier is useful if the input signal is a current.

## 4.9 The Three Basic Amplifier Configurations: Summary and Comparison

Table 6.1 is a summary of die small-signal characteristics of the three amplifier configurations.

**Table 6.1** Characteristics of the three MOSFET amplifier configurations

| Configuration | Voltage gain | Current gain | Input resistance | Output resistance |
|---|---|---|---|---|
| Common source | $A_v > 1$ | — | $R_{TH}$ | Moderate to high |
| Source follower | $A_v \cong 1$ | — | $R_{TH}$ | Low |
| Common gate | $A_v > 1$ | $A_i \cong 1$ | Low | Moderate to high |

The input resistance looking directly into the gate of the common-source and source-follower circuits is essentially infinite at low to moderate signal frequencies. However, the input resistance, of these discrete amplifiers is the Thevenin equivalent resistance $R_{TH}$ of the bias resistors. In contrast, the input resistance to the common-gate circuit is generally in the range of a few hundred ohms.

The output resistance of the source follower is generally in the range of a few hundred ohms. The output resistance of the common-source and common-gate configurations is dominated by the resistance $R_D$. The specific characteristics of these single-stage amplifiers are used in the design of multistage amplifiers.

In the last chapter, we considered three all-MOSFET inverters and plotted the voltage transfer characteristics. All three inverters use an n-channel enhancement-mode driver transistor. The three types of load devices are an n-channel enhancement-mode device, an n-channel depletion-mode device, and a p-channel enhancement-mode device. The MOS transistor used as a load device is referred to as an active load. We mentioned that these three circuits can be used as amplifiers.

In this section, we revisit these three circuits and consider their amplifier characteristics. We will emphasize the small-signal equivalent circuits. This section serves as an introduction to more advanced MOS integrated circuit amplifier designs considered in Part II of the text.

**NMOS Amplifiers with Enhancement Load**

The characteristics of an n-channel enhancement toad device were presented in the last chapter. Figure 6.38(a) shows an NMOS enhancement load transistor.

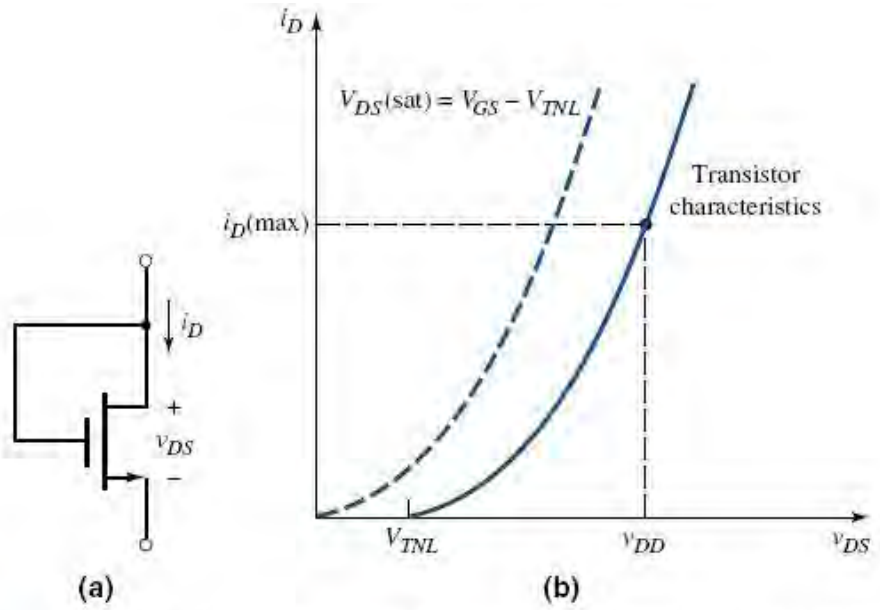
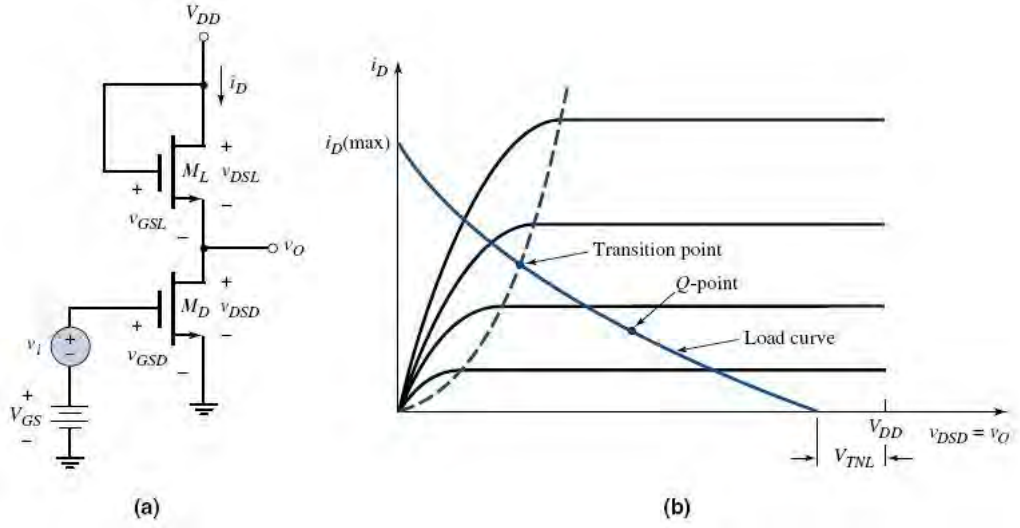



**Figure 6.38** (a) NMOS enhancement-mode transistor with gate and drain connected in a load device configuration and (b) current–voltage characteristics of NMOS enhancement load transistor

and Figure 6.38{b) shows the current-voltage characteristics. The threshold voltage is $V_{TNL}$.

Figure 6.39(a) shows an NMOS amplifier with an enhancement load.



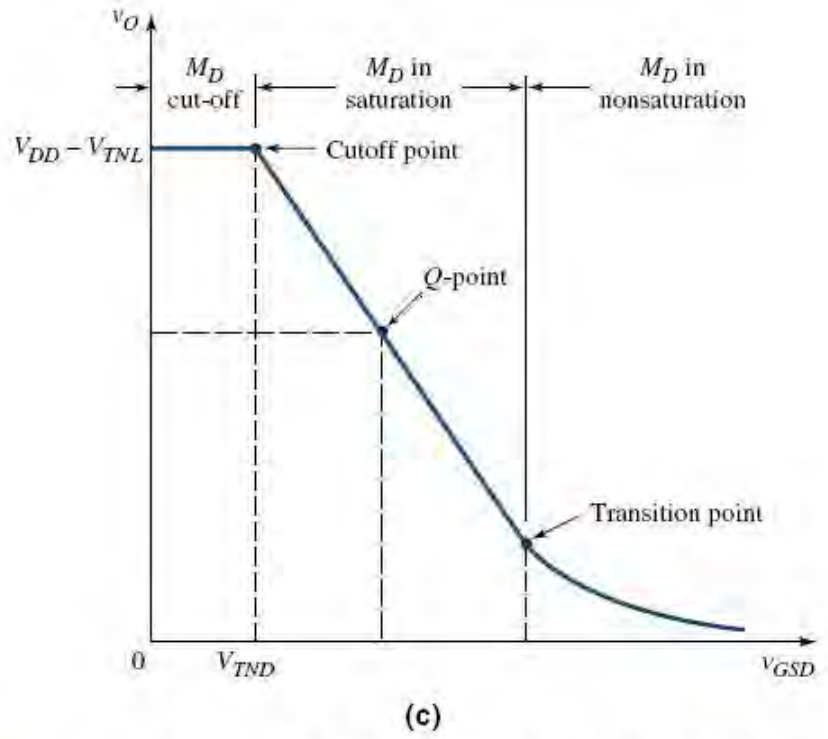



**Figure 6.39** (a) NMOS amplifier with enhancement load device; (b) driver transistor characteristics and enhancement load curve with transition point; and (c) voltage transfer characteristics of NMOS amplifier with enhancement load device

The driver transistor is $M_D$ and the load transistor is $M_L$. The characteristics of transistor $M_D$ and the load curve are shown in Figure 6.39(b). The load curve is essentially the mirror image of the i-v characteristic of the load device. Since the i-v characteristics of the load device are nonlinear, the load curve is also nonlinear. The load curve intersects the voltage axis at $V_{DD} - V_{TNL}$, which is the point where the current in the enhancement load device goes to zero. The transition point is also shown on the curve.

The voltage transfer characteristic is also useful in visualizing the operation of the amplifier. This curve is shown in Figure 6.39(c). When the enhancement-mode driver first begins to conduct, it is biased in the saturation region. For use as an amplifier, the circuit Q-point should be in this region, as shown in both Figures 6.39{b) and (c).

We can now apply the small-signal equivalent circuits to find the voltage gain. In the discussion of the source follower, we found that the equivalent resistance looking into the source terminal (with $R_S = \infty$) was

$R_O = (1 / gm) \parallel r_O$. The small-signal equivalent circuit of the inverter is given in Figure 6.40, where the subscripts D and L refer to the driver and load transistors, respectively. We are again neglecting the body effect of the load transistor.

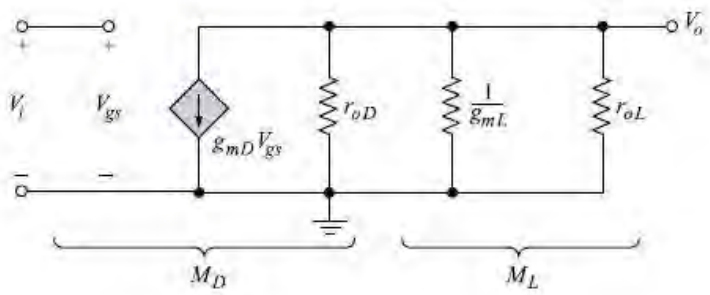



**Figure 6.40** Small-signal equivalent circuit of NMOS inverter with enhancement load device

The small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_{mD}\left(r_{oD} \left\| \frac{1}{g_{mL}} \right\| r_{oL}\right) \tag{6.49}$$

Since, generally, $1/g_{mL} \ll r_{oL}$ and $1/g_{mD} \ll r_{oD}$, the voltage gain, to a good approximation is given by

$$A_v = \frac{-g_{mD}}{g_{mL}} = -\sqrt{\frac{K_{nD}}{K_{nL}}} = -\sqrt{\frac{(W/L)_D}{(W/L)_L}} \tag{6.50}$$

The voltage gain, then, is related to the size of the two transistors.

## 4.10 Recommended Questions

1. Which amplifiers are classified as power amplifiers? Explain the general features of a power amplifier.
2. Give the expression for dc power input, ac power output and efficiency of a series fed, directly, coupled class A amplifier.
3. When the power dissipation is maximum, in class A amplifiers? What is the power dissipation rating of a transistor?
4. Explain with neat circuit diagram, the working of a transformer coupled class A power amplifier.
5. Prove that the maximum efficiency of a transformer coupled class A amplifier is 50%.
6. What is harmonic distortion? How the output signal gets distorted due to the harmonic distortion.
7. Draw a neat circuit diagram of push pull class B amplifier. Explain its working.
8. Draw the circuit diagram of class B push pull amplifier and discuss
    a. Its merits.
    b. Cross-over distortion
9. Prove that the maximum efficiency of a class B amplifier is 78.5%.
10. Write a short note on class D amplifier.
11. Give the classification of multistage amplifier. Explain the various distortions in amplifiers. (July-2007)