

Operational Amplifier Circuits

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Abstract

In this lab we investigate the the properties of operational amplifiers. An operational amplifier takes two electrical inputs along with up to two sources of power and outputs the difference between the two input potentials as the output potential. Utilizing feedback through combinations of resistors and/or capacitors in parallel, the operational amplifier can amplify the output potential or act as more complicated circuit elements like differentiators and integrators which we also investigate. In this lab we measure how these outputs relate to the inputs and power supplies and verify the functionality of these circuit elements.

1 Introduction

Although the internal circuitry is beyond what we will investigate in this lab, at its core, an operational amplifier (hereafter called op-amps) creates a potential at its output terminal proportional to the difference between the two input potentials. A circuit diagram for an ideal op-amp is shown in Figure 1.

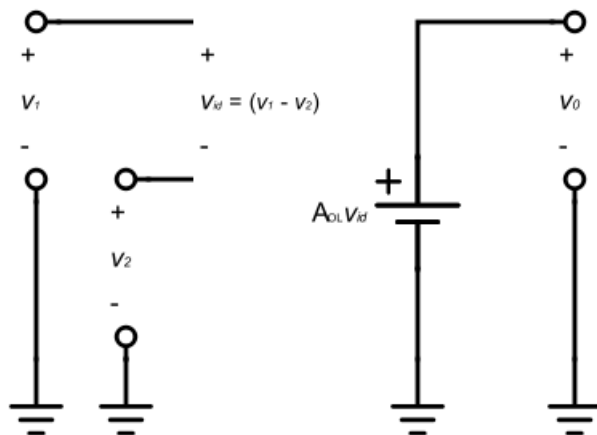


Figure 1: Equivalent circuit for an ideal op-amp. The open-loop gain, A_{OL} is very large.

An op-amp has two input terminals, the non-inverting input and the inverting input. For a voltage of v_1 applied at the non-inverting input and a voltage of v_2 applied at the inverting input, the op-amp will produce at its output terminal a potential equal to the product of the open-loop gain, A_{OL} , and the potential difference between the input voltages, $v_{id} = (v_1 - v_2)$. This can be expressed as $v_0 = A_{OL}(v_1 - v_2)$. The open-loop gain is ideally very large and constant, this will be useful when we implement negative feedback in the circuit as it allows the circuit to satisfy the summing-point constraint for a wide variety of input voltages. For our experiment we use the LM741 op-amp, which has A_{OL} on the order of 2×10^5 . The circuit symbol for the op-amp is shown in Figure 2, the inputs V_{cc} and V_{ee} are the positive and negative power supplies respectively. An op-amp is limited to producing only output voltages within the strict range of $V_{ee} \leq v_0 \leq V_{cc}$.

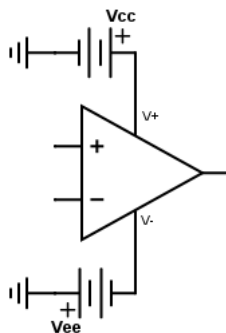


Figure 2: Symbolic representation of an op-amp, including power supplies V_{ee} and V_{cc} .

The basic op-amp circuit we investigate in this lab is called the inverting amplifier, or the basic inverter. The circuit diagram for the basic inverter is shown in Figure 3. It consists of an input potential fed through some input resistor, R_1 , into the inverting input of the op-amp with the non-inverting input leading directly to the ground. The output terminal applies its voltage across some element R_L . Most importantly however is the resistive element linking the output back to the inverting input, R_2 . This element creates what is known as negative feedback, and is the necessary factor in allowing the op-amp to work as an amplifying circuit.

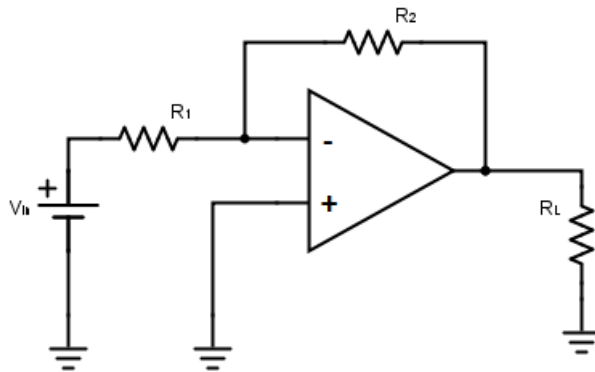


Figure 3: Circuit diagram for the basic inverter, including the input resistance, R_1 , the feedback resistor, R_2 , and the load resistor, R_L .

Because the open-loop gain is very large, any input voltage, V_{in} , no matter how small will result in a large output voltage from the op-amp with opposite polarity with respect to the input. Some of this output voltage is fed through the feedback resistor back to the inverting input terminal. Subsequently, because the output voltage has opposite polarity to the input voltage, the voltage at the inverting input terminal is instantaneously driven towards zero, and over a very short time scale (related to the open-loop gain and other factors internal to the op-amp) it will reach zero exactly. This negative feedback creates what is known as the summing point-constraint, that is, that the potential difference between the input terminals of an ideal op-amp is necessarily zero at all times, provided that negative feedback exists in the circuit.

Since the input voltage is applied across the input resistor, R_1 , we can say from Ohm's law that the current through R_1 is $i_1 = \frac{v_{in}}{R_1}$. But because of the summing-point constraint, the input and output voltages of the op-amp are zero, and so no current may flow through it. Thus the current i_1 can only flow through the feedback resistor, R_2 , so we may say that $i_2 = i_1$. Applying Kirchoff's Voltage Law from ground through the load resistor, then the feedback resistor, across the input terminals, and back to ground (keeping in mind the summing-point constrain), we obtain the relation $v_0 + R_2 i_2 = 0$. Substituting the relation $i_2 = i_1 = \frac{v_{in}}{R_1}$ from earlier we find that

$$\frac{v_0}{v_{in}} = -\frac{R_2}{R_1} = A_v$$

We call A_v the closed-loop gain, and it is the ratio between the voltage across some load and the input voltage when the circuit is closed. Thus we have constructed the simple circuit

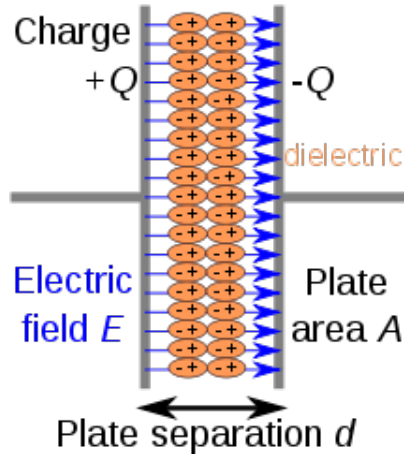


Figure 4: Basic principles of a capacitor. [Source: Wikipedia.org]

known as the basic inverting amplifier.

Before we continue with more complicated circuits, it is necessary to discuss the basic principles of capacitors and their capacitance. Figure 4 shows the basic principles of a capacitor. A capacitor consists of two conducting plates separated by a non-conducting region known as the dielectric. When a voltage is applied across a capacitor, for example by a battery, positive charges are driven towards one plate and negative charges towards the other. However, the charges cannot cross from one plate to another due to the insulating properties of the dielectric. And so, an electric field is created between the plates proportional to the voltage applied across them. This effect can be characterized as such

$$C = \frac{Q}{V}$$

Here Q is the net charge on each plate, V is the voltage applied, and C is known as the capacitance of the capacitor. The capacitance of the capacitor is a function of the area of the plates, their separation, and the electric permittivity of the dielectric. It can be written as

$$C = \epsilon_r \epsilon_0 \frac{A}{d}$$

Here, A is the area of the two plates, d their separation, ϵ_0 the vacuum permittivity, and ϵ_r the relative permittivity of the dielectric. Since current is the time rate of change of charge, we can differentiate the equation above to get the current flowing "through" the capacitor as a function of the voltage

$$I(t) = C \frac{dV(t)}{dt}$$

We say the current flows through the capacitor only to express the motion of charges in the system, in reality charges cannot flow like this due to the insulating nature of the dielectric.

Figure 5 shows the circuit diagram for the basic integrator circuit. Although similar in design an concept to the basic inverting amplifier, the integrator has the effect of producing

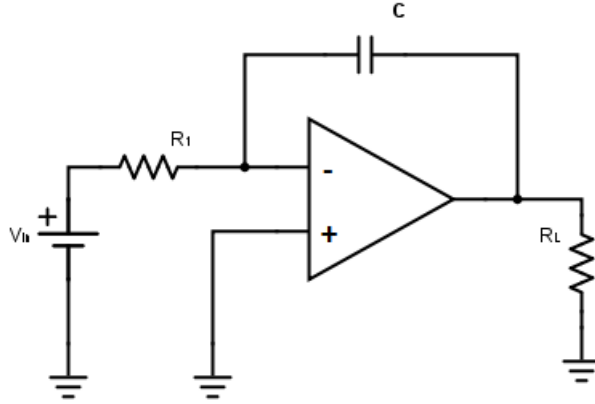


Figure 5: Circuit diagram for the basic integrator, including the input resistance, R_1 , the feedback capacitor, C , and the load resistor, R_L .

an output voltage at its terminal proportional to the time-integral of the input voltage from the time the circuit starts. Like earlier we first look at the current through R_1 as a result of the input voltage, however, it is now helpful to consider some time-dependant voltage $v_{in}(t)$ rather than the steady-state input we considered before. Here we see

$$i_{in}(t) = \frac{v_{in}(t)}{R_1}$$

, and consequently from the summing-point constraint we again see that $i_C(t) = i_{in}(t)$. From our capacitor equation this becomes

$$C \frac{dv_c(t)}{dt} = i_{in}(t)$$

Rearranging this equation and integrating we get

$$v_c(t) = \frac{1}{C} \int_0^t i_{in}(t) dt$$

Applying KVL through the output load, the capacitor, and the input terminals, and keeping in mind the summing-point constraint we obtain $v_0(t) = -v_c(t)$. Substituting our earlier equation we can solve this circuit for its characteristic equation

$$v_0(t) = -\frac{1}{R_1 C} \int_0^t v_{in}(t) dt$$

This shows, as stated earlier, that our integrator circuit produces a voltage proportional to the running-time integral of the input voltage, with the constant of proportionality equal to $-\frac{1}{R_1 C}$.

Figure 6 shows another similar circuit diagram, this time for the basic differentiator circuit. This circuit will produce an output voltage proportional to the time-derivative of

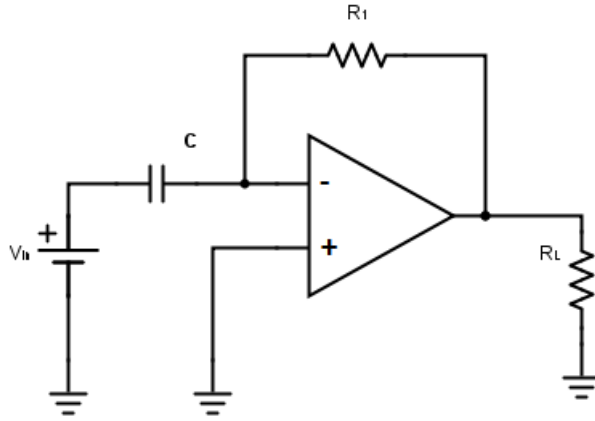


Figure 6: Circuit diagram for the basic differentiator, including the input capacitance, C , the feedback resistor, R_1 , and the load resistor, R_L .

the input voltage. Firstly we look at the current passing through the input capacitance. Since the input voltage is strictly applied across the capacitor and the voltage at the other end is zero due to the summing-point constraint we get that

$$i_{in} = C \frac{dv_{in}(t)}{dt}$$

This then is equal to the current flowing through the feedback resistor, i_r . Application of KVL through the output resistor, the feedback resistor and the input terminals tells us that

$$i_r = -\frac{v_0}{R_1}$$

Combining these equations we get that

$$v_0 = -R_1 C \frac{dv_{in}}{dt}$$

This shows, as stated earlier, that our differentiator circuit produces a voltage proportional to the time-derivative of the input voltage, with constant of proportionality equal to $-R_1 C$.

Lastly, we note that in practicality, an integrator circuit as described above is not necessarily optimal for all inputs. When the frequency of the input voltage is very low, or when the input voltage is a constant (i.e. a frequency of zero), our integrator circuit will produce a voltage that is ever growing, and it will continue to grow until the voltage reaches in magnitude the power supply voltage. This is not a particularly useful property of an integrator, so, in practice we attach a large resistor across the capacitor. This has the effect of turning the integrator into a basic inverting amplifier when the input frequency is low. This drives the output voltage back towards zero, and prevents the output from reaching saturation, and when the frequency is higher, due to the high resistance of the resistor, the functionality of the integrator is not particularly impaired.

2 Experiment

2.1 DC Amplification

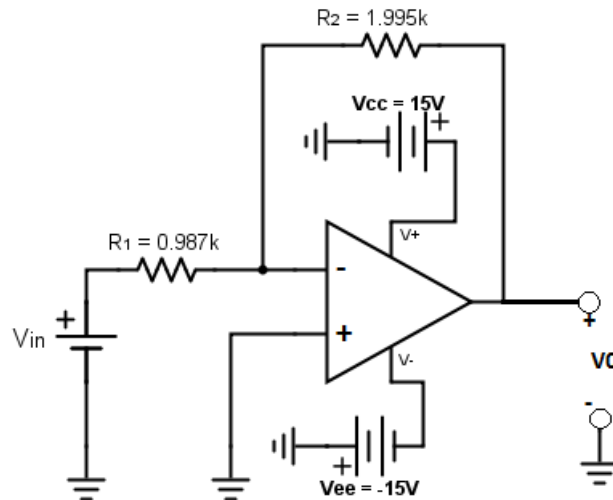


Figure 7: Circuit diagram for the first experiment.

A circuit was constructed according to the diagram in Figure 7. By inspection we see that this is identical to the basic inverting amplifier circuit we described before. Thus we expect to see a voltage gain of $A_v = \frac{R_2}{R_1} = 2.021$. Applying a DC voltage at V_{in} and varying it from -5V to +5V we observe across V_0 voltages as found in Table 1.

We then expanded our data to include voltages from -10V to +10V. This continued data is found in Table 2.

Inverting Amplifier	
V_{in} (Volts)	V_0 (Volts)
-5	-9.896
-4	-7.916
-3	-5.939
-2	-3.958
-1	-1.974
0	0.000
1	1.969
2	3.950
3	5.930
4	7.911
5	9.893

Table 1: Voltage across the output terminal vs. input voltage for the basic inverting amplifier.

Inverting Amplifier	
V_{in} (Volts)	V_0 (Volts)
-10	-13.949
-9	-13.960
-8	-13.972
-7	-13.846
-6	-11.871
6	11.868
7	13.245
8	13.227
9	13.209
10	13.191

Table 2: Expanded voltage across the output terminal vs. input voltage for the basic inverting amplifier.

Then we set our source voltage to $V_{in} = 3V$. We measured the current through the input resistor, and we measured it to be 4.355 mA.

2.2 AC Amplification with Integrators and Differentiators

We then switched our DC voltage source out for an AC voltage source, and set $v_{in} = 1\text{Volt}$ with frequency of 100 Hz. A peak to peak time difference of $\delta t = 5\text{ms}$ was observed between v_{in} and v_0 .

Next we increased the amplitude of the 100 Hz input voltage to $v_{in} = 8\text{Volts}$. We observed that the output voltages reached saturation at each peak at a value of around $v_{max} = \pm 14.2\text{Volts}$.

We then switched out the input resistor with one of size $R_1 = 9.958k\Omega$ and our feedback resistor with a capacitor of capacitance $C = 0.1\mu F$. This then creates an integrator with constant of proportionality $-\frac{1}{RC} = 996 \times 10^{-6}$. Refer to Figure 5 for the circuit diagram of such a circuit. We observe that as the frequency of our input voltage increases, that the magnitude of the output voltage decreases.

We then varied the frequency of the input voltage, f , and measured the ratio of the output voltage magnitude to the input magnitude as $G = \frac{v_0}{v_{in}}$. This data can be seen in Table 3. Next we observed the phase shift between the output and input voltages as a function of frequency. This data can be seen in Table 4.

Integrator Circuit	
f (Hz)	G (unitless)
100	1.438
200	0.775
300	0.538
400	0.405
500	0.330
600	0.280
700	0.240
800	0.208
900	0.185
1000	0.168
2000	0.0863
3000	0.0600
4000	0.0435

Table 3: Frequency response of the integrator circuit.

Integrator Circuit	
f (Hz)	ϕ (degrees)
100	96.74°
500	92.31°
1000	91.55°
3000	94.66°
5000	89.06°
7000	90.71°
10000	88.57°

Table 4: Phase change vs. frequency of the integrator circuit.

Next, we then switched our input resistor and feedback capacitor with each other This then created a differentiator with constant of proportionality $-RC = 0.996 \times 10^{-3}$. Refer to Figure 6 for the circuit diagram of such a circuit. We observe that as the frequency of our input voltage increases, that the magnitude of the output voltage increases.

We then varied the frequency of the input voltage, f , and measured the ratio of the output voltage magnitude to the input magnitude as $G = \frac{v_o}{v_{in}}$. This data can be seen in Table 5. Next we observed the phase shift between the output and input voltages as a function of frequency. This data can be seen in Table 6.

Integrator Circuit	
f (Hz)	G (unitless)
100	0.635
200	1.231
300	1.846
400	2.462
500	3.077
600	3.846
700	4.423
800	5.000
900	5.577
1000	6.154
2000	12.212
3000	13.558
4000	13.558

Table 5: Frequency response of the integrator circuit.

Integrator Circuit	
f (Hz)	ϕ (degrees)
100	-88.39°
500	-89.86°
1000	-91.96°
3000	-136°
5000	-161.2°
7000	-130°
10000	-101.2°

Table 6: Phase change vs. frequency of the integrator circuit.

3 Results

3.1 DC Amplification

From the first experiment, we can plot our initial data. This plot is shown in Figure!!!!!!!. Applying linear regression to this plot, we find that V_0 is correlated with V_{in} by $V_0 = 1.978V_{in}$. This slope of 1.978 corresponds to the closed-loop gain A_v that we calculated earlier to be $A_v = 2.021$. These values are quite close, off by only 2.1%.

From our continued data from this experiment, we can plot again as shown in Figure!!!. Note that the output voltages reach a cap of around ± 13.5 Volts. This is because, due to the amplification, our circuit is attempting to output voltages near or higher than the voltages supplied by our power supplies. This cause voltage saturation, which is exactly what we see in the plot.

By measuring the current through R_1 when an input voltage of V_{in} is applied, we can determine that input resistance via Ohm's law as $R_1 = \frac{V_{in}}{i_R} = \frac{3V}{4.355mA} = 689\Omega$.

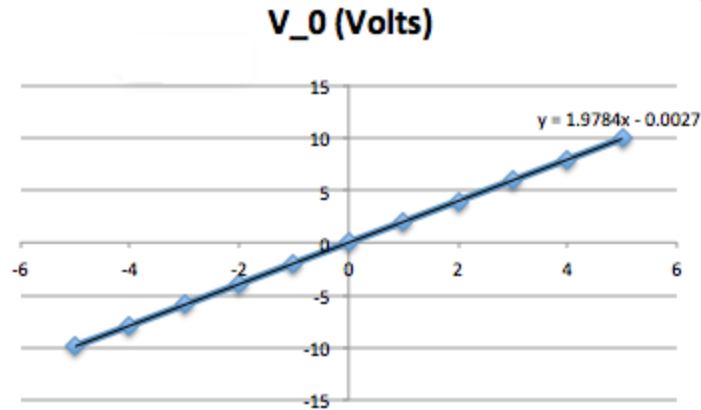


Figure 8: Plot of V_0 vs V_{in} for the first experiment.

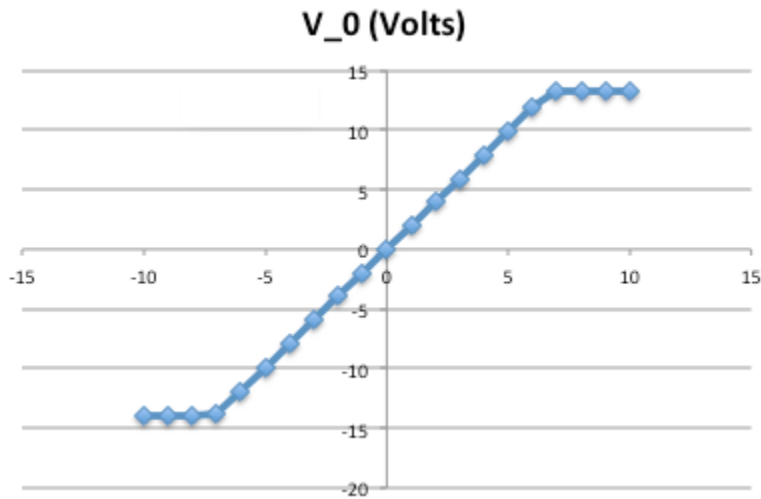


Figure 9: Expanded plot of V_0 vs V_{in} for the first experiment.

3.2 AC Amplification with Integrators and Differentiators

Seeing a time difference of 5 ms peak to peak implies a phase difference between the input and output voltages. Using the relation $\phi = 2\pi f\delta t$ we determine that $\phi = 3.14159 \approx \pi$. This makes sense because a signal inversion can also be considered to merely apply a phase change of π .

The saturation of output voltage for an input voltage of 8V makes sense because amplification would drive the output voltage towards 16V, however the power supplies limit the output voltage tow within $V_{ee} \leq v_0 \leq V_{cc}$, which is exactly what we see.

Plotting our values of $20\log(G)$ vs. $\log(f)$ for our integrator circuit we get the plot as shown in Figure !!! . Note that this plot scales linearly and negatively. Since we expect the output voltage to be $v_0(t) = -\frac{1}{R_1C} \int_0^t v_{in}(t)dt$, we can substitute in $v_{in} = A\sin(2\pi ft)$. Taking this and integrating we get the relation $v_0(t) = -\frac{K}{f}v_{in}$, where K is a combination of several constants. Dividing by v_{in} and taking the log of both sides we get $\log(\frac{v_0}{v_{in}}) = G = K_2\log(f)$,

which is a linear equation, and is exactly what we see in the plot. We note that for each frequency of measurement, we always measured a phase shift of around $+\frac{\pi}{2}$. Note that when integrating a sine wave, one finds a negative cosine wave. This is equivalent to shifting the phase forwards by $+\frac{\pi}{2}$, which is exactly what we see here.

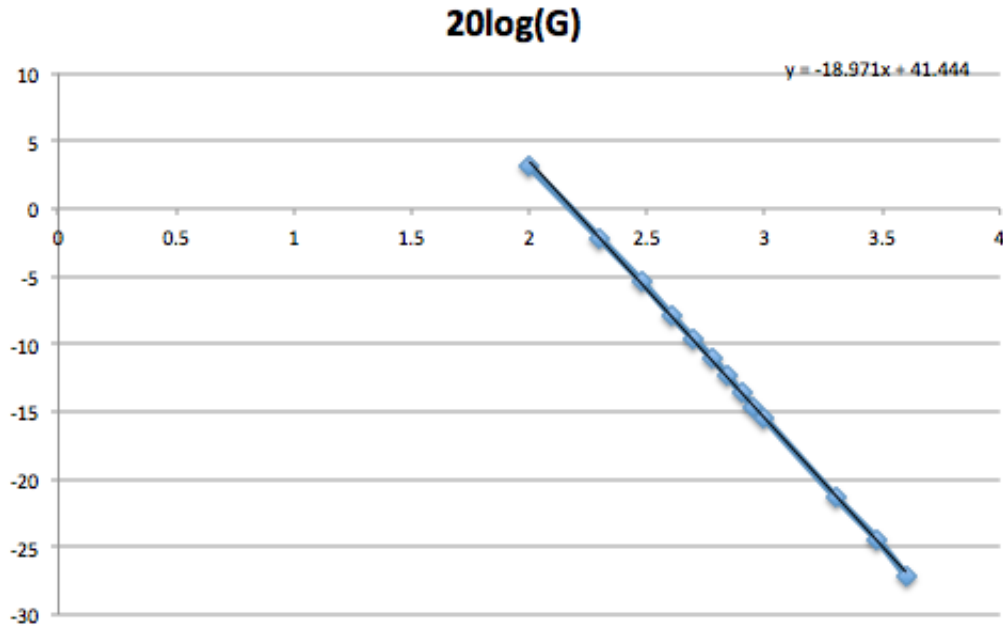


Figure 10: Plot of $20\log(G)$ vs $\log(f)$ for the second experiment integrator.

Plotting our values of $20\log(G)$ vs. $\log(f)$ for our differentiator circuit we get the plot as shown in Figure !!! . Note that this plot scales linearly and positively. Since we expect the output voltage to be $v_0(t) = -R_1C\frac{v_{in}(t)}{dt}$, we can substitute in $v_{in} = A\sin(2\pi ft)$. Taking this and differentiating we get the relation $v_0(t) = Kfv_{in}$, where K is a combination of several constants. Dividing by v_{in} and taking the log of both sides we get $\log(\frac{v_0}{v_{in}}) = G = K_2\log(f)$, which is a linear equation, and is exactly what we see in the plot. We note that for each frequency of measurement, we always measured a phase shift of around $-\frac{\pi}{2}$. Note that when differentiating a sine wave, one finds a positive cosine wave. This is equivalent to shifting the phase backwards by $-\frac{\pi}{2}$, which is exactly what we see here.

4 Conclusions

Our experiments on a basic inverting amplifier were a rousing success. We found that the open-loop gain was exactly expected, to within just a few percent. We found that the behavior of the amplifier was as expected, output voltage scaled linearly with the input voltage, up until the output voltage would approach the supply voltage, at which point the output voltage became saturated as expected.

Our experiments on integrators and differentiators were also successful. We found that our integrator outputted a voltage that was the time integral of our input voltage. We found

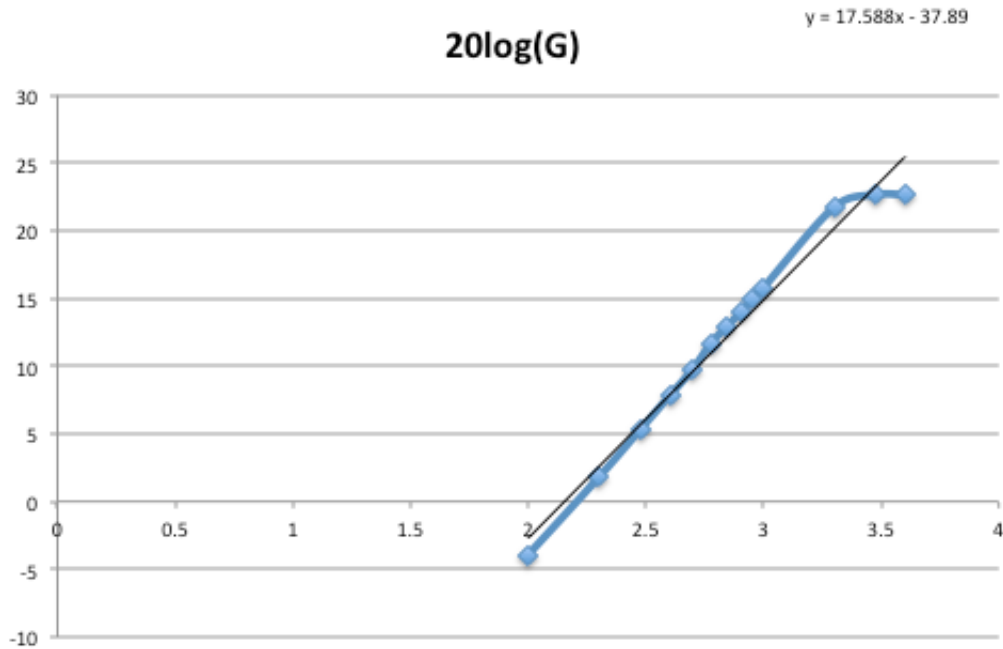


Figure 11: Plot of $20\log(G)$ vs $\log(f)$ for the second experiment differentiator.

that the frequency response of our integrator caused voltages to drop as frequency increased, which is exactly what you would expect. We found that the phase shift of our integrator was to shift the function forward by $\frac{\pi}{2}$, which is equivalent to the integrand operator acting on a sinusoidal wave.

We found that our differentiator outputted a voltage that was the time derivative of our input voltage. We found that the frequency response of our differentiator caused voltages to increase as frequency increased, which is exactly what you would expect. We found that the phase shift of our differentiator was to shift the function backward by $\frac{\pi}{2}$, which is equivalent to the differential operator acting on a sinusoidal wave.