International Journal of Engineering and Applied Sciences (IJEAS)
ISSN: 2394-3661, Volume-4, Issue-5, May 2017 (Approved by University Grants Commission, India)

GDI: Power efficient and less transistor count technique for logic designs

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***Abstract*— GDI, i.e., Gate Diffusion Input is the latest technology for the designing of VLSI circuits. Comparing it to other designing techniques such as CMOS and PTL, GDI is considered as more efficient technique. GDI technique consumes less power, less area and it also has lower complexity of designing. Performance of any circuit is based on its delay, power and the area, and GDI is the technique in which all the above three constraints are maintained with respect to other designing techniques. This paper gives the comparative study if GDI and other techniques with respect to area , power consumed ,delay and complexity of design. This paper also gives the advantages of GDI.**

***Index Terms*— GDI, CMOS, PTL, complexity of design**

I. INTRODUCTION

With the advance research in IC technology integration of more devices on a single chip is possible. This helps in reducing area. GDI is a technique which is suitable for design of fast, low power circuits using reduced number of transistors compared to traditional CMOS designs. PTL(pass-transistor logic) is also one of the logic that is popular in low power circuits. The basic disadvantage behind the PTL is at reduced power supply it gives slow operation and high input voltage level at the regenerative inverter is not V_{dd} , the PMOS device in the inverter is not fully turned off and hence direct path static power dissipation is significant[1]. So as compared to traditional CMOS design and existing PTL technique GDI technique is more suitable for fast and low power circuits using less transistors.

The aim of this paper is to compare the GDI technique with other traditional techniques and the give the difference in power dissipation and area.

Transistor count is a primary concern which largely affects the design complexity of larger circuit. For submicron CMOS technology area, topology selection, power dissipation and speed are very important aspect for high speed and low power application. These issues can be overcome by incorporating Gated Diffusion Input (GDI) technique[2].

The organization of the paper is as follows: Section 1 briefs the introduction, Section 2 describes the basic GDI cell and its design ,Section 3 gives the comparison of GDI technique with other techniques Section 4 presents the advantages of GDI, Section 5 gives simulation and results and lastly Section 6 gives Conclusion.

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II. BASIC GDI CELL

The Gate diffusion Input is based on the use of a simple cell . At first look the basic GDI cell reminds of CMOS inverter but there is difference between two

- The GDI cell contains three inputs G(common gate input of NMOS and PMOS),P(input to the source/drain of PMOS), and N(input to the source/drain of PMOS)
- Bulks of both NMOS and PMOS are connected to Nor P(respectively), so it can be arbitrarily biased at contrast with a CMOS inverter[1].

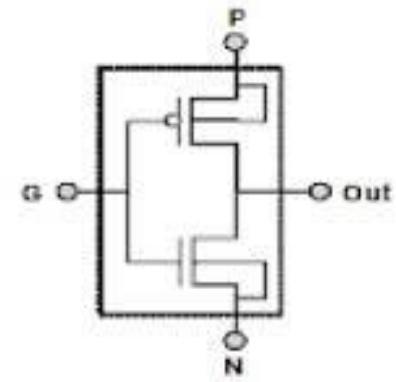

Fig1: Basic GDI Cell

Here from the GDI cell a simple change in the input can lead to six different functions. These functions are very hard to implement in traditional designing techniques but s way more easier in GDI designing technique . Most of the methods are based in F1 and F2 functions.

Six different Boolean functions are:

- N=0, P=B, G=A OUT=$\bar{A}$B (FUNCTION F1)
- N=B, P=1 ,G=A OUT=$\bar{A}$+B (FUNCTION F2)
- N=1, P=B, G=A OUT=A+B (OR FUNCTION)
- N=B ,P=0, ,G=A OUT=AB (AND FUNCTION)
- N=0, P=1, G=A OUT=$\bar{A}$ (NOT FUNCTION)

III. COMPARISON OF GDI WITH OTHER TECHNIQUES.

A. Power dissipation due to hazards and critical race conditions, leakage and direct path currents, power consuming transitions in unused circuitry and pre-charge transistors. A fast arithmetic operation requires fast circuit and the fast circuits require small size to minimize the delay effects of wires. Small size implies a single chip implementation, to minimize wire de- lays, and to make it possible to implement these fast circuits as part of a larger single chip system to minimize input/output delays [5].Performance

criteria for logic styles are circuit speed, circuit size, power

dissipation, and wiring complexity as well as ease-of-use and generality of gates in cell-based design techniques[7].

GDI technique uses less complex designs hence results in less number of devices , less area, less delay, and less power dissipation.

TABLE II gives the design layout of the different logic techniques

TABLE I

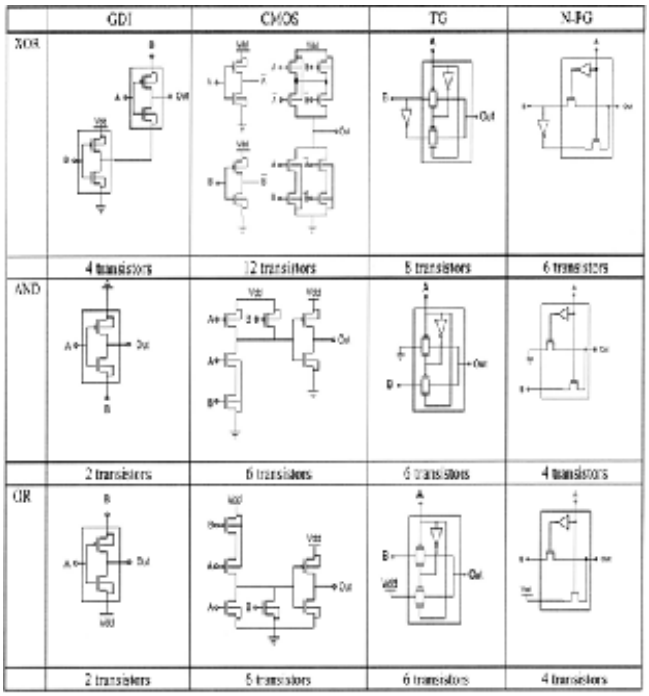

TABLE III gives the comparison of various designing techniques with respect to transistor count ,delay and power consumption.

TABLE III

FEATURES	CSL	CPL	DPL	GDI
TRANSISTORS COUNT	HIGH	LOW	LOW	VERY LOW
DELAY	HIGH	VERY LOW	VERY HIGH	LOW
POWER CONSUMPTION	VERY HIGH	LOW	HIGH	VERY LOW

IV. ADVANTAGES OF GDI

The major advantage of GDI technique is less transistor count. As we can see that MUX design is a complex design which by CMOS logic requires 8-12 transistors and requires only 2 transistors in case of GDI design.

Table 4 gives the comparison of transistor count of static CMOS and GDI

TABLE 4

FUNCTION	GDI	CMOS
INVERTER	2	2
OR	2	6
AND	2	6
MUX	2	12
XOR	4	16
XNOR	4	16
NAND	4	4
NOR	4	4

V. SIMULATION RESULTS

Here in this section different gates are simulated using PSPICE. Gates are designed by both using CMOS and GDI, both are compared by their power dissipation

A. AND GATE

```
NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(   1)    0.0000  (   2)    5.0000  (   3)    4.9991  (   4)    0.0000
(   5)    4.9991  (   6) 21.73E-12


VOLTAGE SOURCE CURRENTS
NAME         CURRENT

VDD         -4.999E-05
VINA         0.000E+00
VINB         0.000E+00

TOTAL POWER DISSIPATION   2.50E-04  WATTS
```

Fig:2 Simulation results of AND gate using CMOS

```
NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(   1)    0.0000  (   2)    0.0000  (   3)    1.4884  (   4)    5.0000


VOLTAGE SOURCE CURRENTS
NAME         CURRENT

VDD         -8.532E-12
VA           0.000E+00
VB           0.000E+00

TOTAL POWER DISSIPATION   4.27E-11  WATTS
```

Fig:3. Simulation results of AND gate using GDI technique

B. OR GATE

```
NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(   1)    0.0000  (   2)    5.0000  (   3)    4.9991  (   4)    0.0000
(   5)    4.9991  (   6) 21.73E-12


VOLTAGE SOURCE CURRENTS
NAME         CURRENT

VDD         -4.999E-05
VINA         0.000E+00
VINB         0.000E+00

TOTAL POWER DISSIPATION   2.50E-04  WATTS
```

Fig :4 Simulation result of OR gate using CMOS

```
NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(   1)    0.0000  (   2)    0.0000  (   3)    1.4884  (   4)    5.0000


VOLTAGE SOURCE CURRENTS
NAME         CURRENT

VDD         -1.354E-11
VIN1         0.000E+00
VIN2         7.033E-12

TOTAL POWER DISSIPATION   6.77E-11  WATTS
```

Fig 6:Simulation result of OR gate using GDI

C. XOR GATE

```
NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(   1)    0.0000  (   2)    0.0000  (   3)-486.6E-15  (   4) 86.89E-12
(   5) 43.45E-12  (   6)    5.0000  (   7)    5.0000  (   8)    5.0000
(   9)    5.0000  (  10)    5.0000


VOLTAGE SOURCE CURRENTS
NAME         CURRENT

VDD         -2.004E-11
VA           0.000E+00
VB           0.000E+00

TOTAL POWER DISSIPATION   1.00E-10  WATTS
```

Fig:7 Simulation result of XOR gate using CMOS

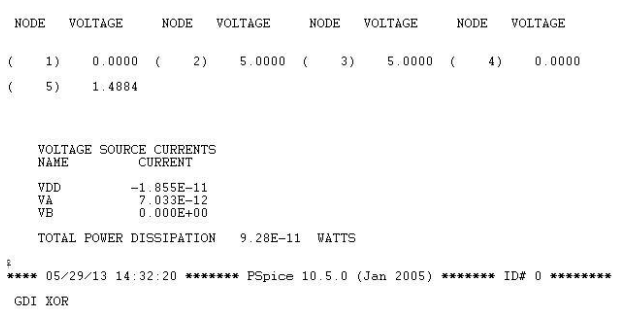

Fig: 8 Simulation result of XOR gate using GDI

Table 5 shows the comparison of power dissipation of CMOS and GDI technique with respect to different gates.

TABLE 5

GATES/CIRCUIT	CMOS	GDI
NOT	2.51E-11	2.51E-11
AND	2.50E-04	4.27E-11
OR	2.50E-04	6.77E-11
XOR	1.00E-10	9.28E-11

VI. CONCLUSION

In this paper GDI technique was presented. The GDI technique allows use of a simple and efficient design algorithm, based on the Shannon expansion[1]. Here in this by the result of simulation we can say that power dissipation is less in the GDI technique compared to CMOS technique. Here we have also seen that transistor count is less in GDI technique compared to other techniques .So in today's digital era use of GDI technique is much more efficient than other techniques.

ACKNOWLEDGEMENT

The authors are thankful to Hon'able C – VI, Dr. AseemChauhan (Additional President, RBEF and Chancellor AUR, Jaipur), Maj. General K. K. Ohri (AVSM, Retd.) Pro-VC Amity University, Uttar Pradesh Lucknow, Wg. Cdr. Dr. Anil Kumar, Retd.(Director, ASET), Prof. S. T. H. Abidi (Professor Emeritus), Brig. U. K. Chopra, Retd.(Director AIIT), for their motivation, kind cooperation, and suggestions.

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