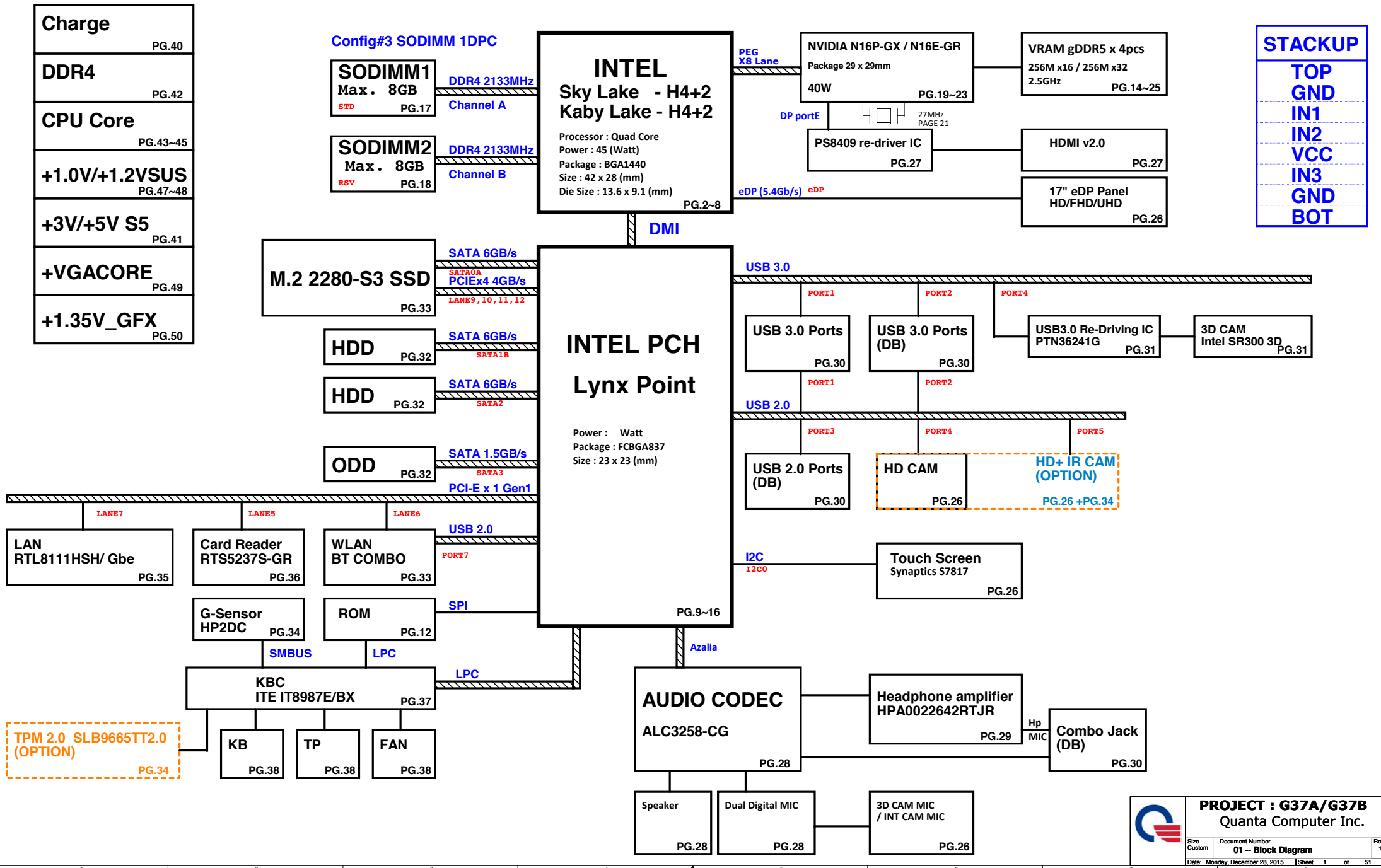


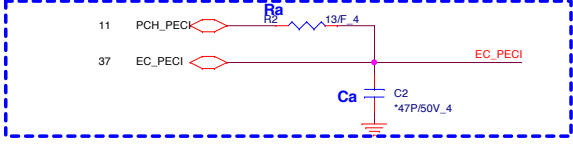
# POWER PAVILION PARFAIT INTEL SKL / KABY -H SYSTEM DIAGRAM 01



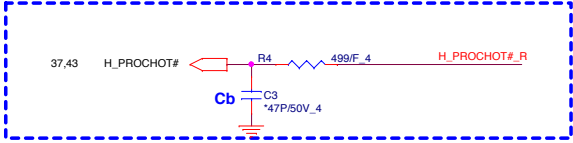
SKYLAKE Processor (CLK, MISC, JTAG)

+1.0V 5,6,10,16,37,48  
+VCCSTPLL 6,43,47

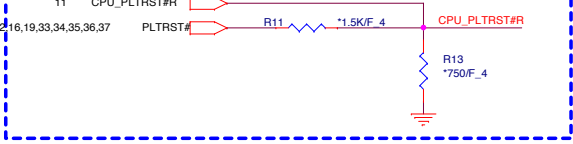
**H\_PECI (50ohm)**  
Trace Length: <0.5 inches  
Ra,Ca need placement close to PCH.



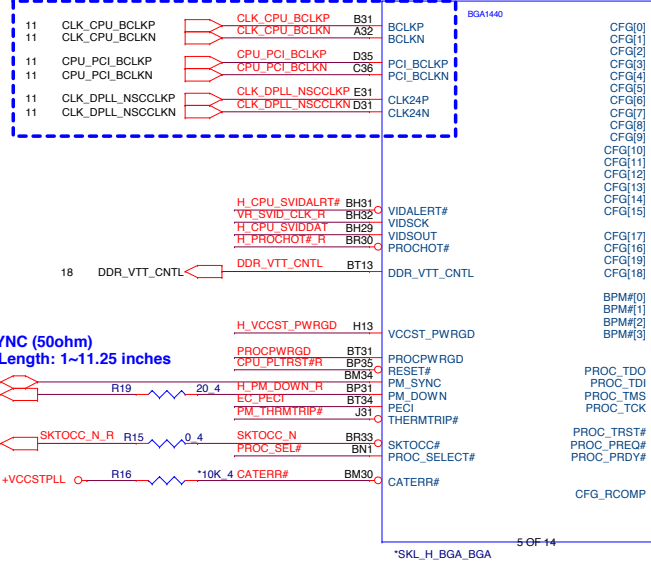
**PROCHOT# (50ohm)**  
Trace Length <11 inches  
Cb need placement near VR



**CPU\_PLTRST# (50ohm)**  
Trace Length: 10~17 inches



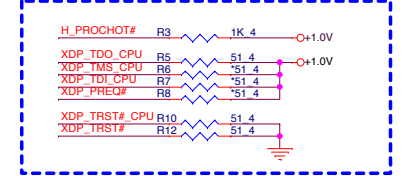
**Host CLK:**  
Trace length < 11000 mils  
Trace spacing = 15 / 20 mils, Impedence 85 ohm



CFG[0]	BN25	CFG0	CFG0	16
CFG[1]	BN27	CFG1	CFG1	16
CFG[2]	BN26	CFG2	CFG2	8,16
CFG[3]	BN28	CFG3	CFG3	8,16
CFG[4]	BR20	CFG4	CFG4	8,16
CFG[5]	BM20	CFG5	CFG5	8,16
CFG[6]	BT20	CFG6	CFG6	8,16
CFG[7]	BR23	CFG7	CFG7	16
CFG[8]	BR22	CFG8	CFG8	16
CFG[9]	BT23	CFG9	CFG9	16
CFG[10]	BT23	CFG10	CFG10	8,16
CFG[11]	BT22	CFG11	CFG11	16
CFG[12]	BM19	CFG12	CFG12	8,16
CFG[13]	BR19	CFG13	CFG13	8,16
CFG[14]	BP19	CFG14	CFG14	16
CFG[15]	BT19	CFG15	CFG15	16
CFG[16]	BN23	CFG16	CFG16	16
CFG[17]	BP23	CFG17	CFG17	16
CFG[18]	BP22	CFG18	CFG18	16
CFG[19]	BN22	CFG19	CFG19	16
BPM#[0]	BR27	XDP_BPM0	XDP_BPM0	16
BPM#[1]	BT27	XDP_BPM1	XDP_BPM1	16
BPM#[2]	BM31	XDP_BPM2	TP2	
BPM#[3]	BT30	XDP_BPM3	TP1	
PROC_TDO	BT28	XDP_TDO_CPU	XDP_TDO_CPU	16
PROC_TDI	BL32	XDP_TDI_CPU	XDP_TDI_CPU	16
PROC_TMS	BP26	XDP_TMS_CPU	XDP_TMS_CPU	16
PROC_TCK	BR28	XDP_TRST#_CPU	XDP_TRST#_CPU	16
PROC_TRST#	BP30	XDP_TRST#	XDP_TRST#	15,16
PROC_PREQ#	BL30	XDP_PREQ#	XDP_PREQ#	15,16
PROC_PRDY#	BP27	XDP_PRDY#	XDP_PRDY#	15,16
CFG_RCOMP	BT25	CFG_RCOMP	CFG_RCOMP	16

Design Note(CFG\_RCOMP):  
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

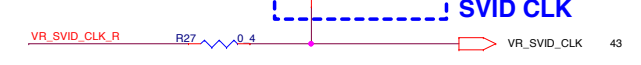
Processor pull-up (CPU)



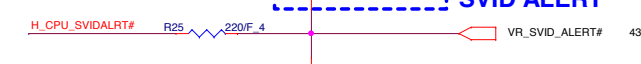
CPU CORE SVID

Layout note:  
1. Need routing together  
2. ALERT need between CLK and DATA.

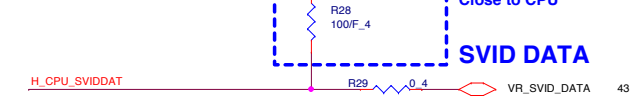
PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE



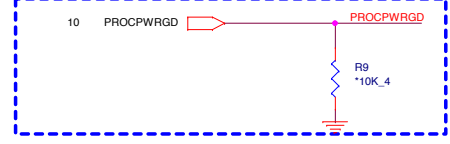
CLOSE TO CPU  
PLACE THE PU RESISTORS



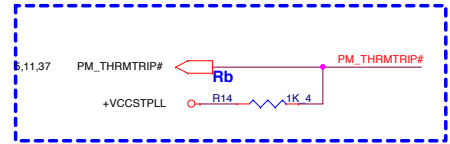
CLOSE TO CPU  
PLACE THE PU RESISTORS



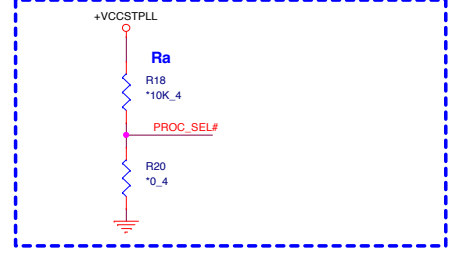
PROCPWRGD (50ohm)  
Trace Length: 1~11.25 inches



THERMTRIP# (50ohm)  
Trace Length: 1.1~12 inches  
Rb need placement near PCH

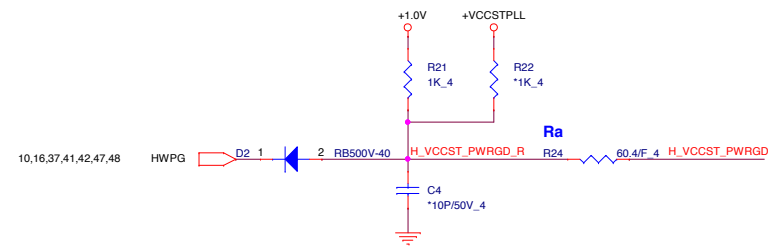


Ra(R10804) Not install in SKL-H



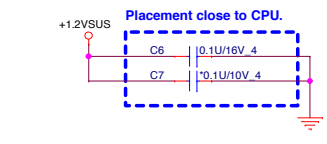
HWPDP

Ra close to CPU side  
H\_VCCST\_PWRGD trace 0.3" - 1.5"



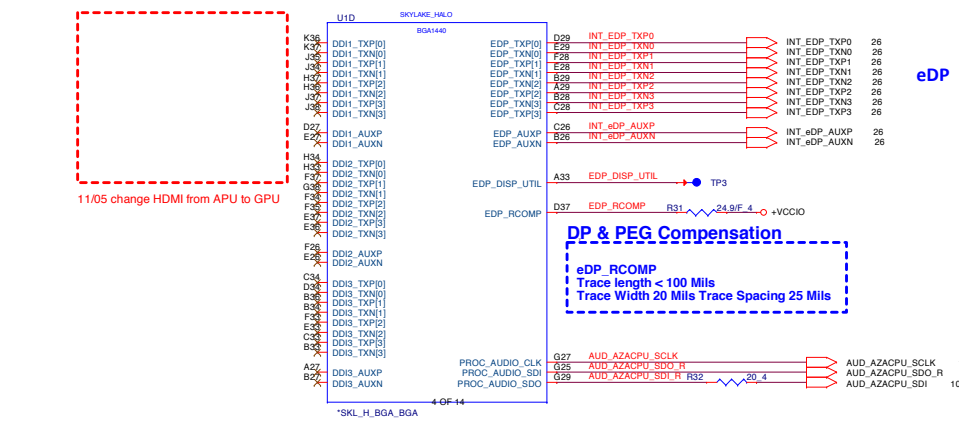
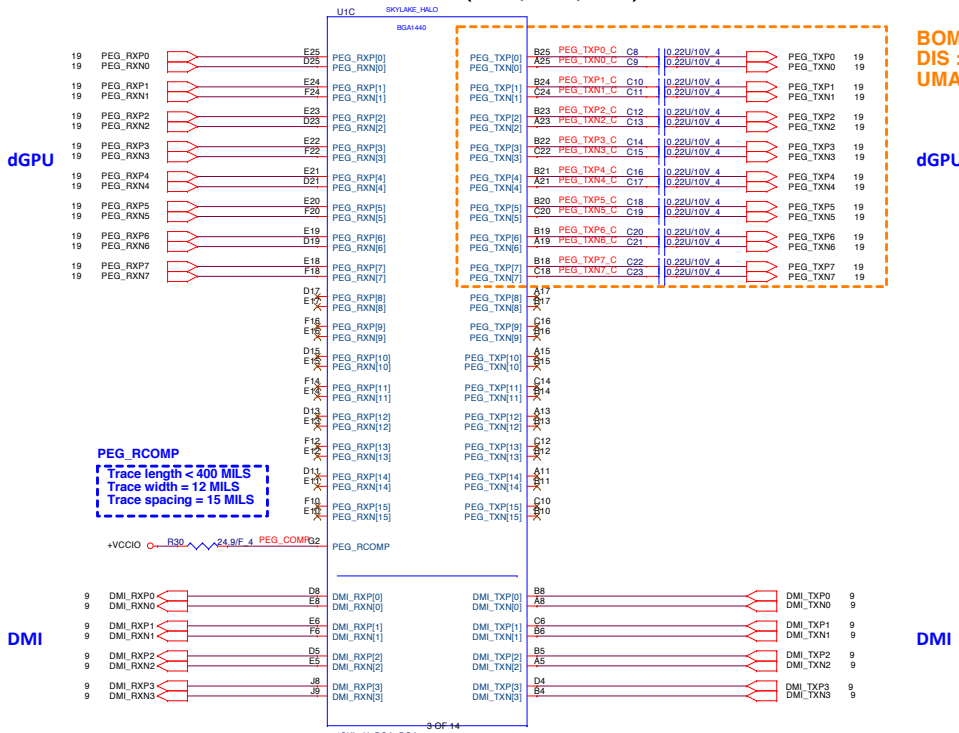
CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A



<p><b>PROJECT : G37A/G37B</b> Quanta Computer Inc.</p>		
Size Custom	Document Number <b>02 - SKL 1/7 (JTAG/MISC)</b>	Rev 1A
Date: Monday, December 28, 2015	Sheet	2 of 51

SKYLAKE Processor (DMI, PEG, FDI)



**PROJECT : G37A/G37B**  
Quanta Computer Inc.

Size Custom	Document Number 03 -- SKL 2/7 (DMI/EDP/PEG)	Rev 1A
Date: Monday, December 28, 2015		Sheet 3 of 51



+3VPCU 10,30,33,37,38,40,41  
 +3V 9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49  
 +1.0V 2,6,10,16,37,48  
 +VCCGT 7,43,45

### SKYLAKE Processor (POWER)

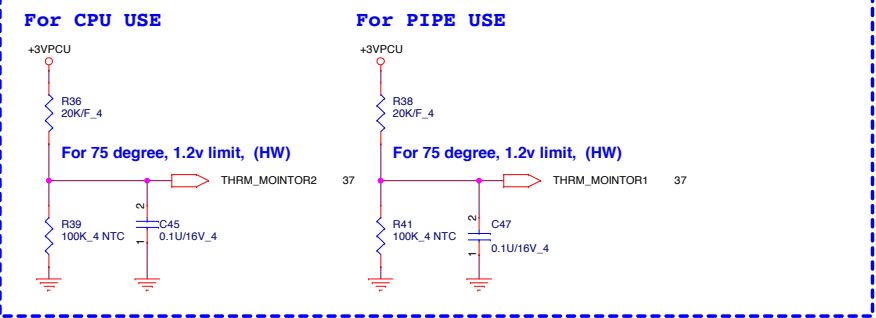
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

1123 Change C27, C29, C33 PN and FP from 0805 to 0603  
 1022 Change C27, C29, C33 PN and FP from 0603 to 0805

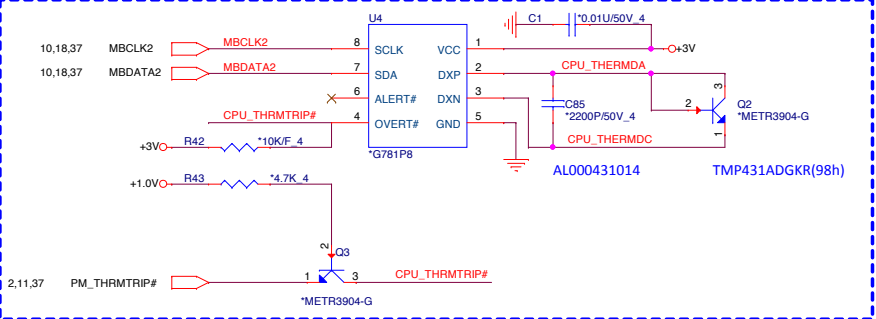


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### IO Thrm Protect Location need thermal confirm



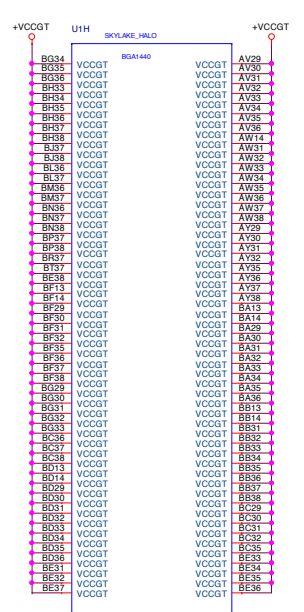
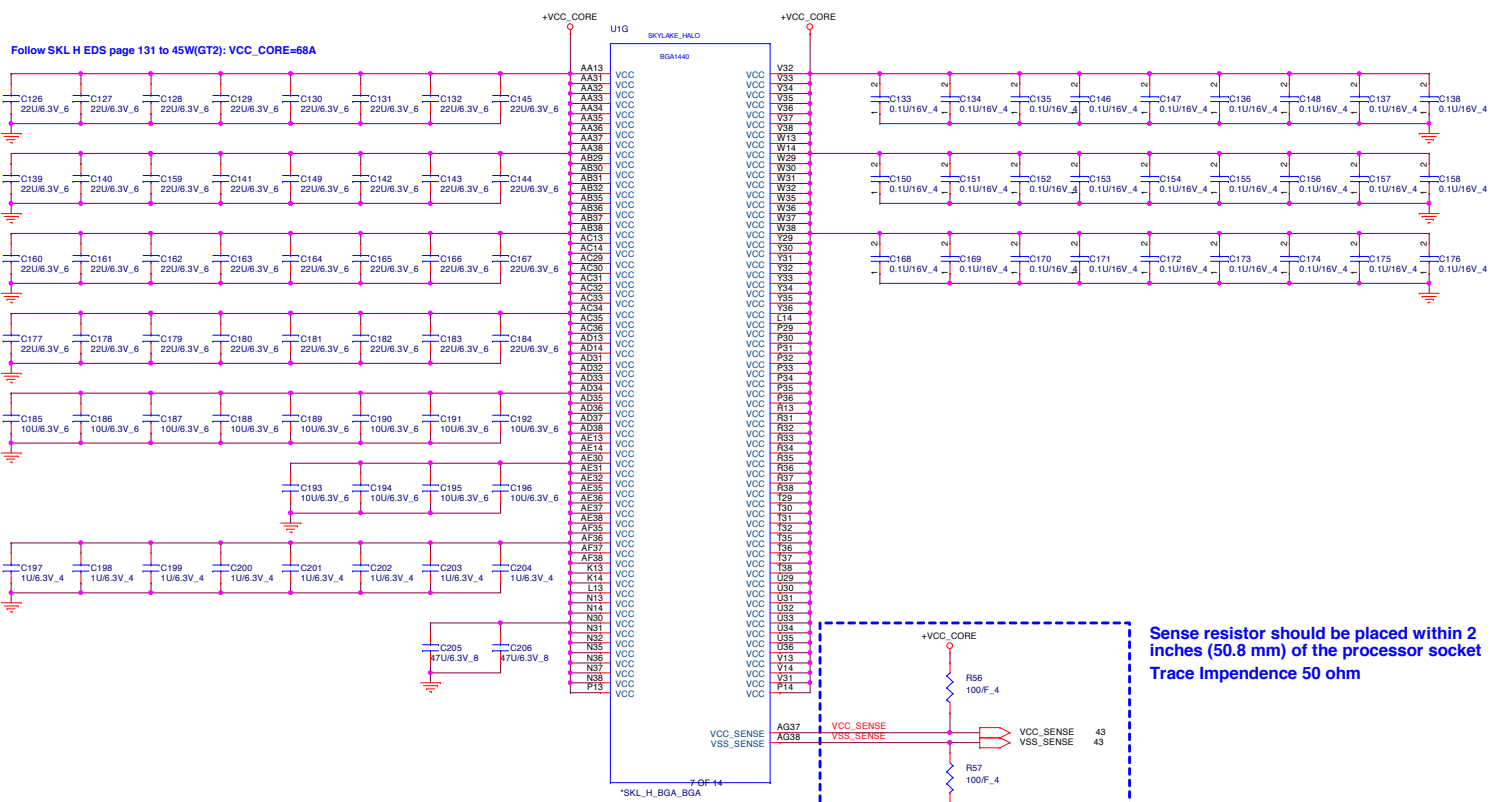
### CPU Thermal Sensor Location need thermal confirm



	<b>PROJECT : G37A/G37B</b>	
	Quanta Computer Inc.	
	Size Custom	Document Number 05 - SKL 4/7 (POWER)
Date: Monday, December 28, 2015   Sheet 5 of 51		



+VCC\_CORE 44  
+VCCGT 5,43,45



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket  
Trace Impedance 50 ohm

		<b>PROJECT : G37A/G37B</b>		Rev 1A
		Quanta Computer Inc.		
Size Custom	Document Number	07 - SKL 6/7 (POWER&GND)		
Date: Monday, December 28, 2015		Sheet	7	of 51









+3V 5,9,10,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49  
+1.0V\_DEEP\_SUS 10,14,16,47,49

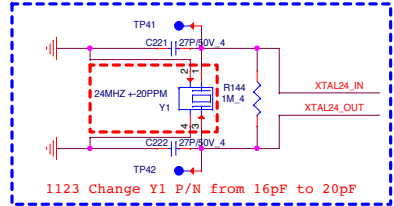
HSIO MUX PORT	
PCIe1-4	NC
PCIe5	Cardreader
PCIe6	Wlan
PCIe7	Lan
PCIe8	NC
PCIe9/SATA0A	SSD PCIe x 4
PCIe10	
PCIe11	
PCIe12	
PCIe13	NC
PCIe14	HDD-1
PCIe15	HDD-2
PCIe16	ODD
PCIe17	NC
PCIe18-20	NC

SSD PCIe x4 LANE

HDD-1 (SATA1B 6Gb/s)

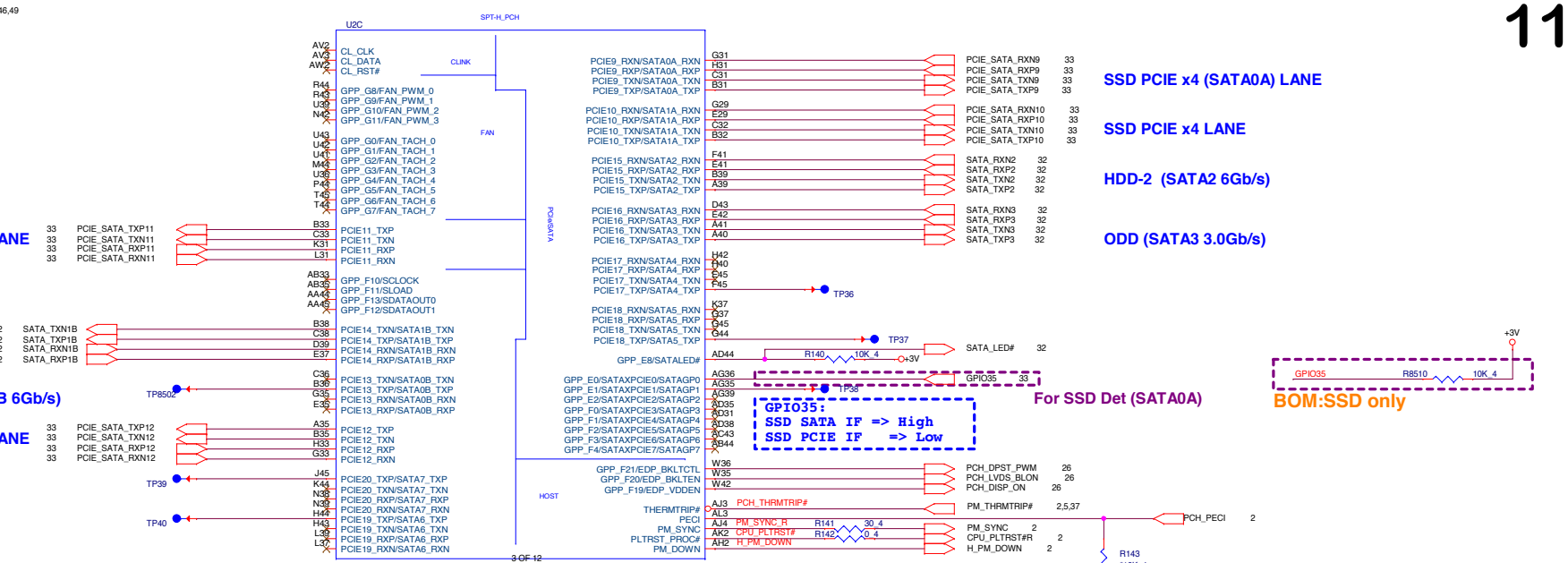
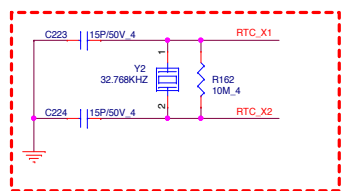
SSD PCIe x4 LANE

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.



Crystal Components with Surrounding 10 mil Wide GND Shield Trace Break Out:4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHZ



SSD PCIe x4 (SATA0A) LANE

SSD PCIe x4 LANE

HDD-2 (SATA2 6Gb/s)

ODD (SATA3 3.0Gb/s)

For SSD Det (SATA0A)

BOM:SSD only

PCH\_DPST\_PWM 26  
PCH\_LVDS\_BLOW 26  
PCH\_DISP\_ON 26

PM\_THRMTRIP# 2,5,37  
PM\_SYNC 2  
CPU\_PLTRST#R 2  
H\_PM\_DOWN 2

PCH\_PECI 2

Card Reader

WLAN

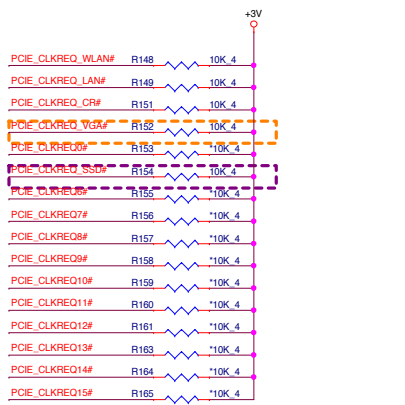
LAN

VGA

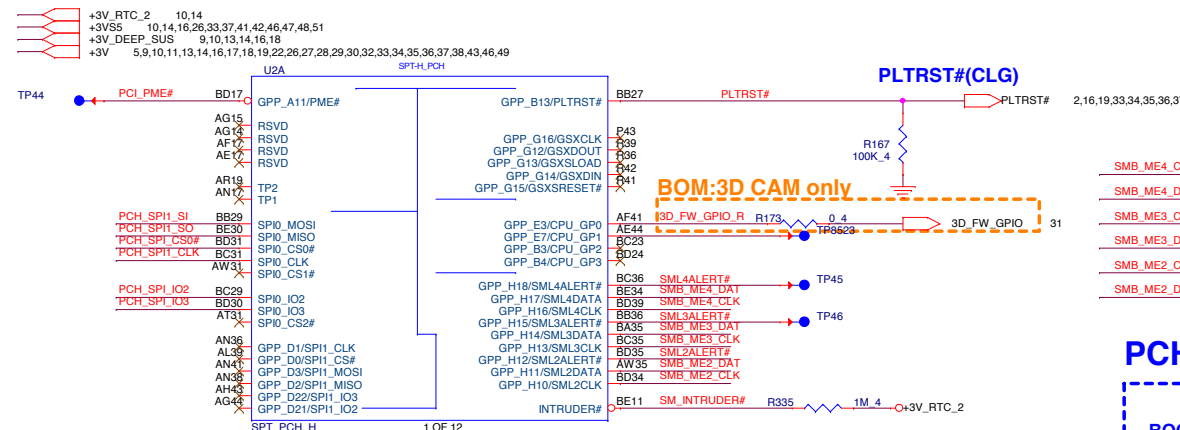
SSD

BOM:DIS only

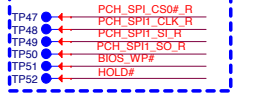
BOM:SSD only



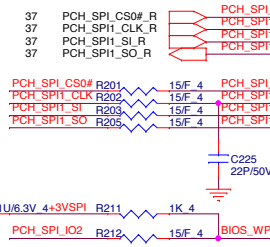
<b>PROJECT : G37A/G37B</b> <b>Quanta Computer Inc.</b>		
Size Custom	Document Number 11 -- PCH 3/7 (SATA/LPC/CLK)	Rev 1A
Date: Monday, December 28, 2015	Sheet 11	of 51



**PCH SPI ROM(CLG)**

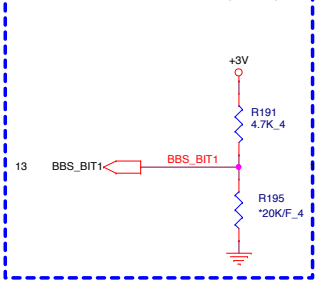


**Place to BOT**

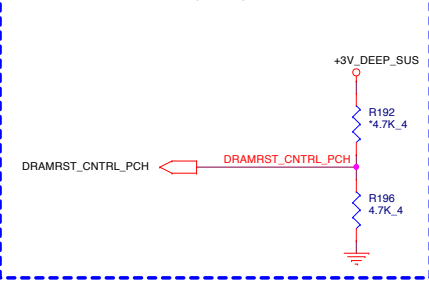


Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE2EZN0Q00(GD25B64CSIGR)
Socket		DFHS08FS023

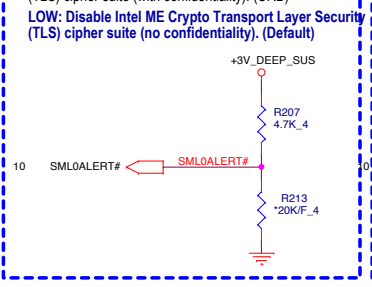
**NO REBOOT IF SAMPLED HIGH**  
 HIGH:TOP SWAP ENABLED (CRB)  
 LOW: Disable "No Reboot" mode. (Default)



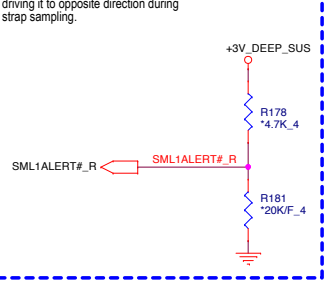
**ESPI/LPC SELECT STRAP**  
 HIGH:ESPI is selected for EC.  
 LOW: LPC is selected for EC. (Default)



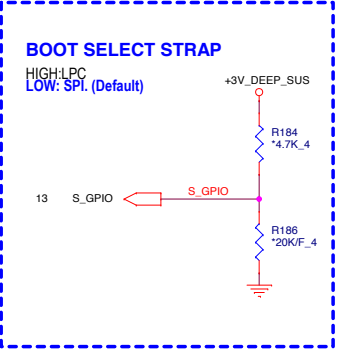
**TLS CONFIDENTIALITY ENABLED**  
 HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)  
 LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)



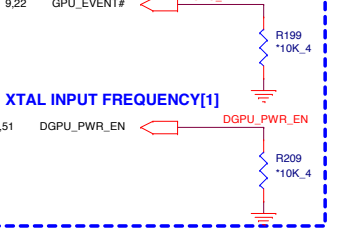
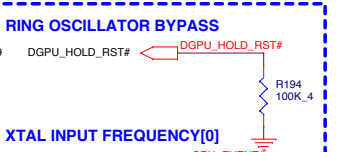
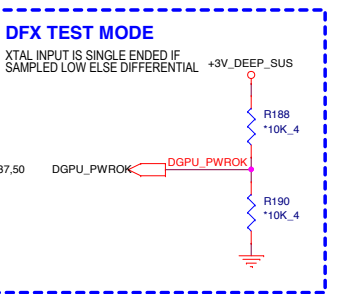
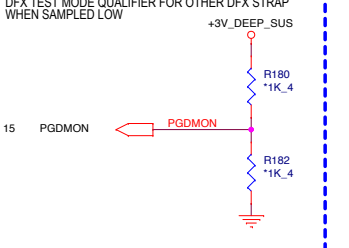
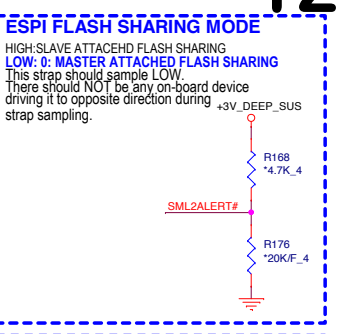
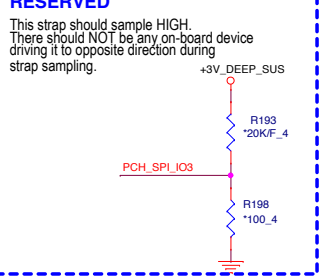
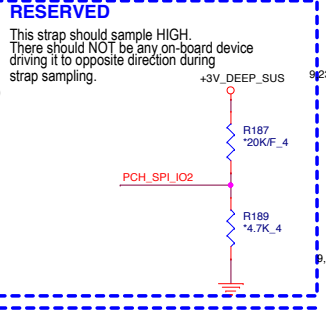
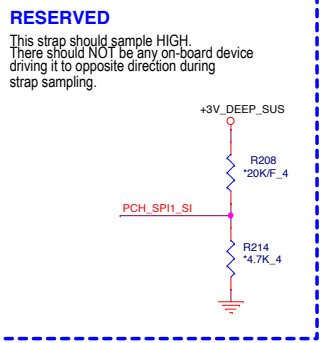
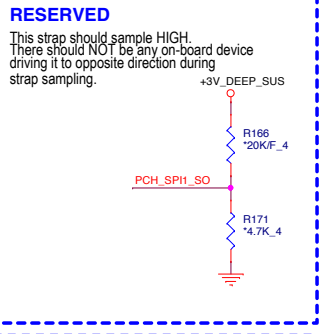
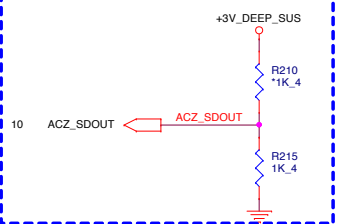
**RESERVED**  
 This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.



**PCH Strap Pin**



**TLS CONFIDENTIALITY ENABLED**  
 HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. (CRB)  
 LOW: security measures defined in the Flash Descriptor. (Default)

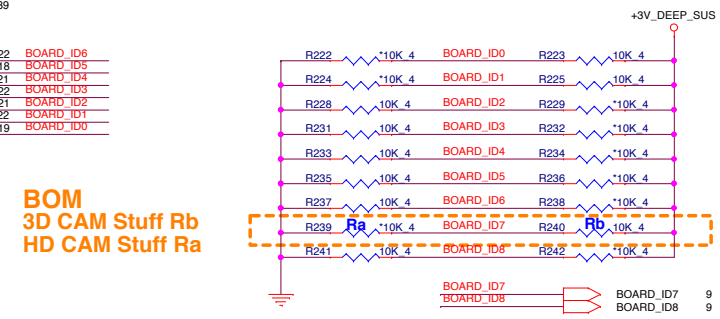
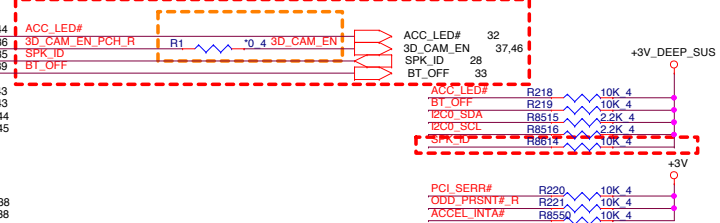
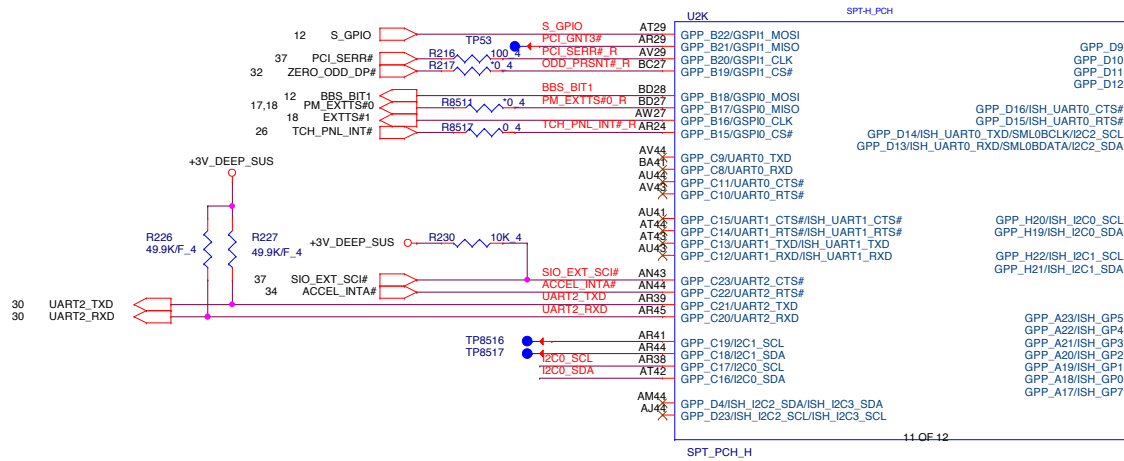


**PROJECT : G37A/G37B**  
 Quanta Computer Inc.

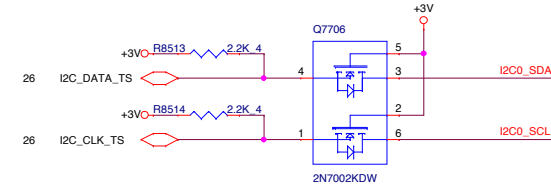
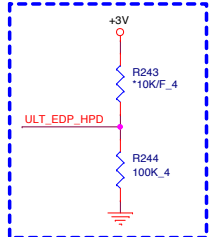
Size Custom	Document Number 12 - PCH 4/7 (GPIO/MISC)	Rev 1A
Date: Monday, December 28, 2015	Sheet 12 of 51	

1123 Change PCH GPP\_D11 Net name from RF\_OFF to SPK\_ID and PUI0K to +3V\_DEEP\_SUS for SPK Vendor ID used

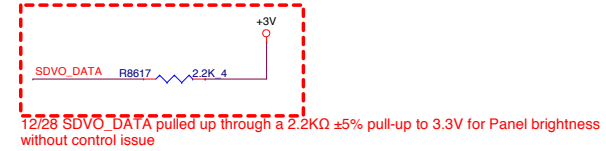
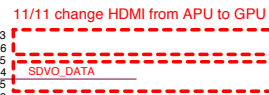
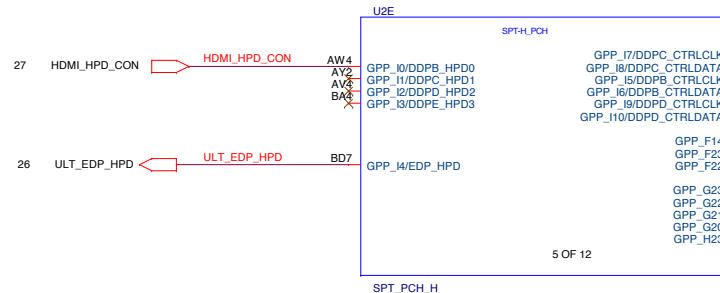
**3D CAMERA**  
BOM: 3D CAM Un-Stuff (EN will from EC control)



Reserve EDP\_HPD opposites circuit!



This signal has a weak internal pull-down.  
0 = Port C and D is not detected.  
1 = Port C and D is detected.

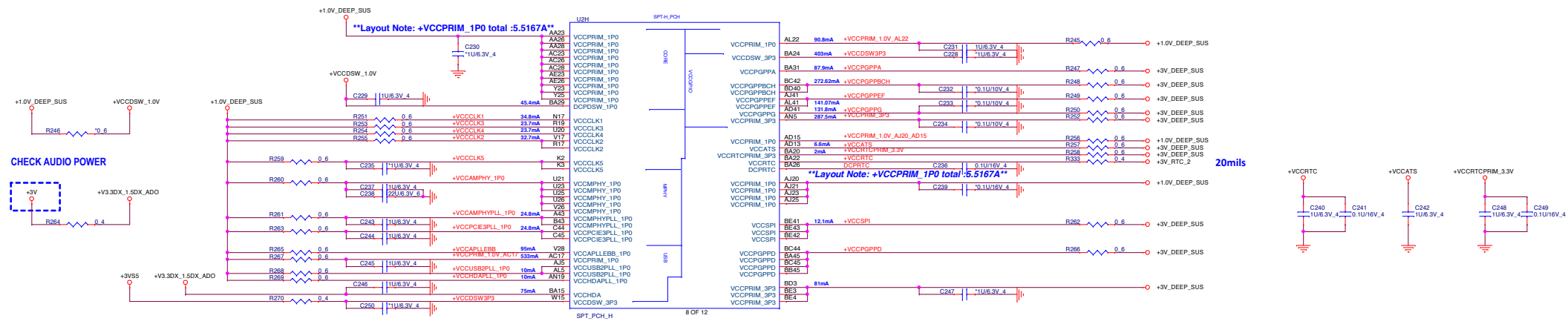


Model	BOARD_ID[8:7] ID8;ID7	BOARD_ID[6:5] ID6;ID5	Board ID [4:3] ID4;ID3	BOARD_ID[2:1] ID2;ID1	BOARD_ID0
Definition	00 Non 3D CAM 01 3D CAM	00 Reserved	Reserved	00 15" P SKL H 01 17" P SKL H 10 17" SP SKL H 11 17" KBL H	0 UMA 1 DIS

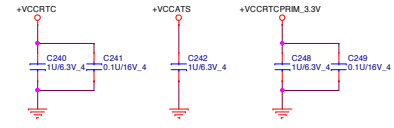
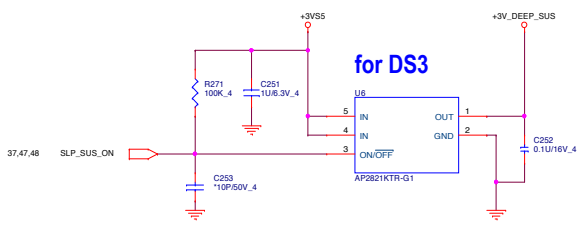
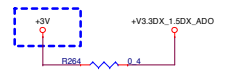
**PROJECT : G37A/G37B**  
Quanta Computer Inc.

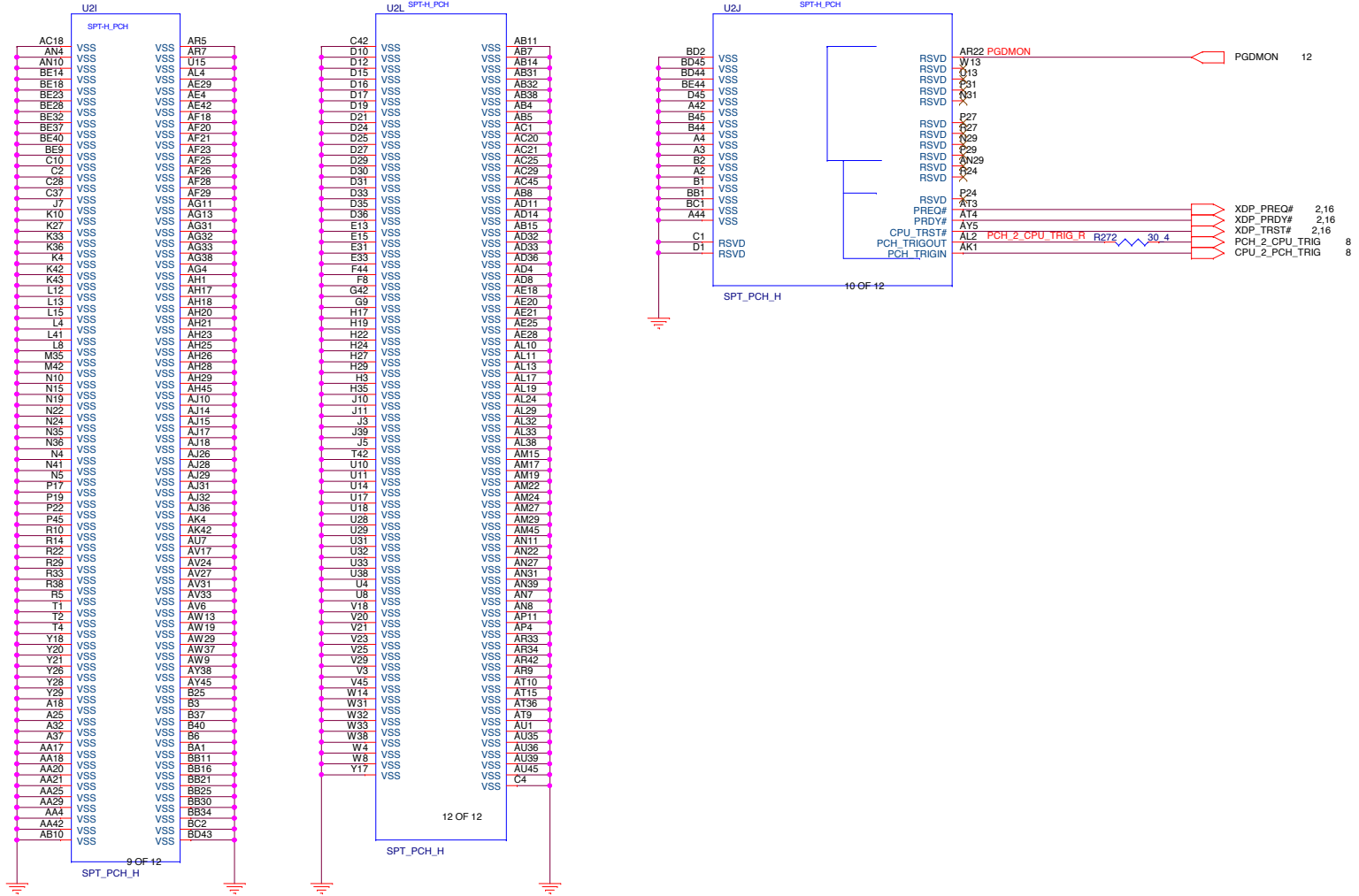
Size Custom	Document Number 13 - PCH 5/7 (GPIO)	Rev 1A
Date: Monday, December 28, 2015	Sheet 13 of 51	


+3V_RTC_2	10,12
+3V55	10,12,16,26,33,37,41,42,46,47,48,51
+3V_DEEP_SUS	6,10,12,13,16,19
+3V	5,9,10,11,12,13,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49
+1.0V_DEEP_SUS	10,11,16,47,48



CHECK AUDIO POWER

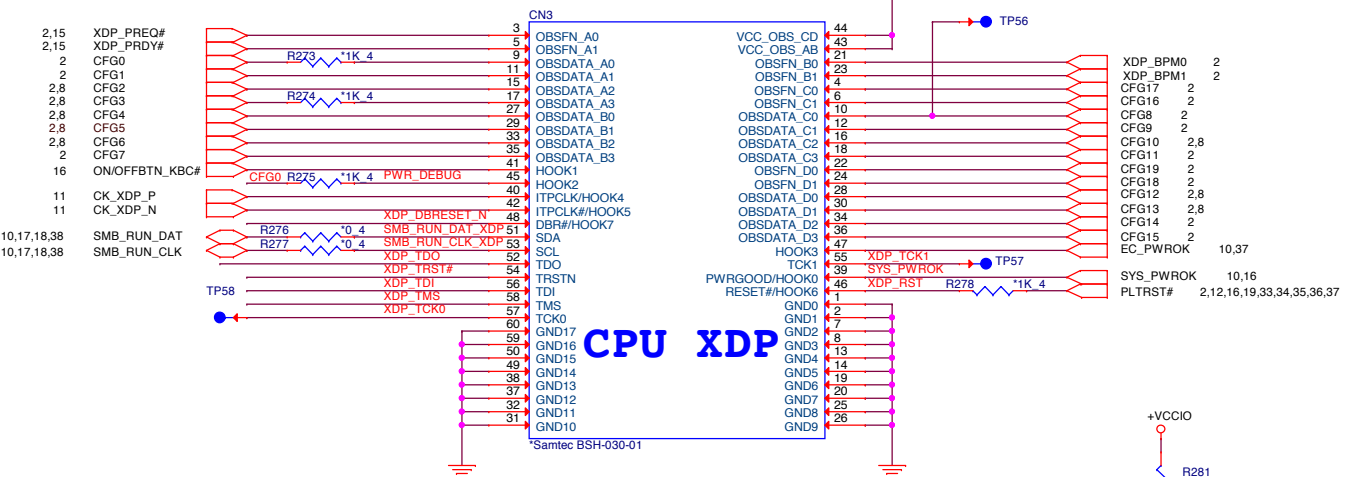




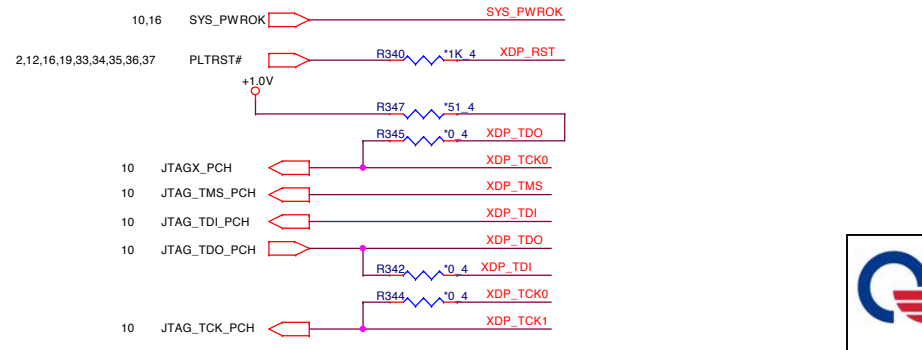
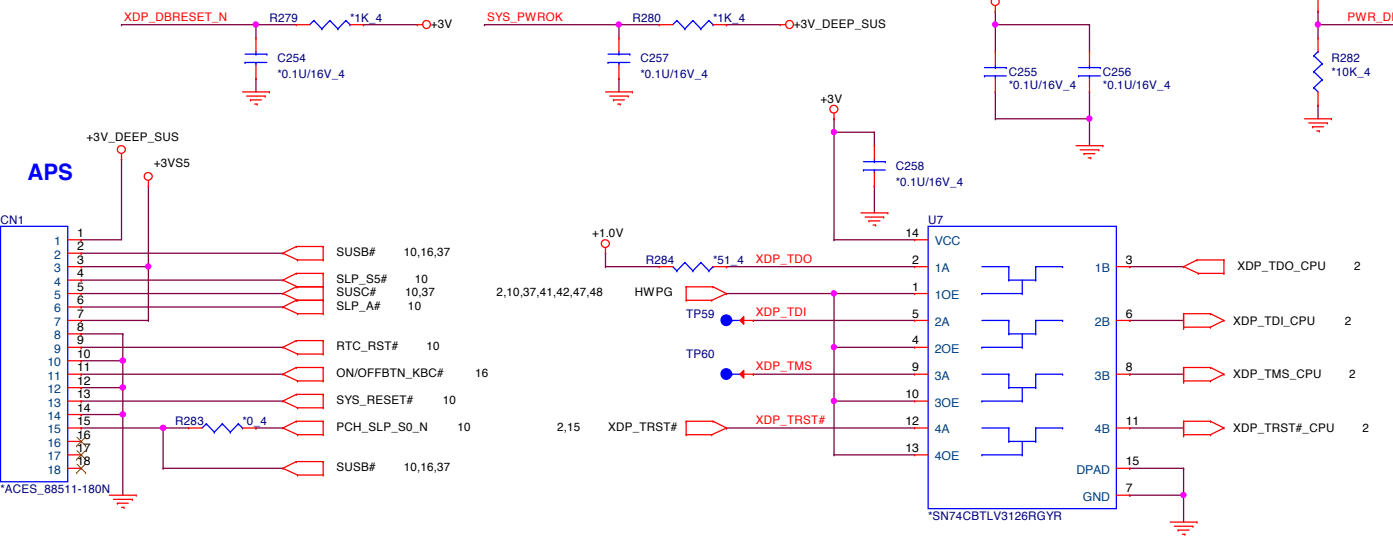
	<b>PROJECT : G37A/G37B</b>		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number 15 - PCH 7/7 (GND)	
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1123 Change XDP Circuit from I to NI

+3VS5	10,12,14,26,33,37,41,42,46,47,48,51
+3V_DEEP_SUS	9,10,12,13,14,18
+3V	5,9,10,11,12,13,14,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49
+1.0V_DEEP_SUS	10,11,14,47,48
+VCCIO	3,6,48
+1.0V	2,5,6,10,37,48



CPU XDP

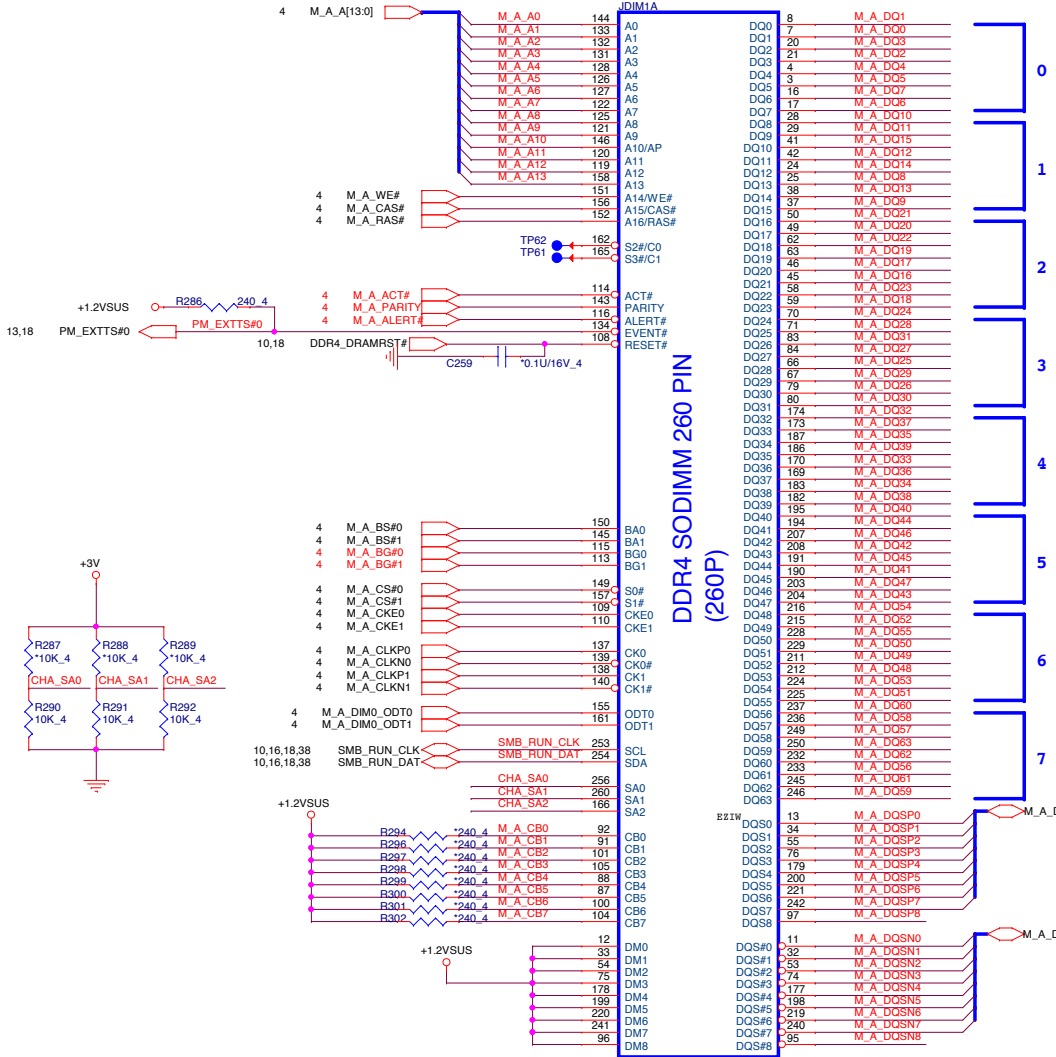


**PROJECT : G37A/G37B**  
 Quanta Computer Inc.

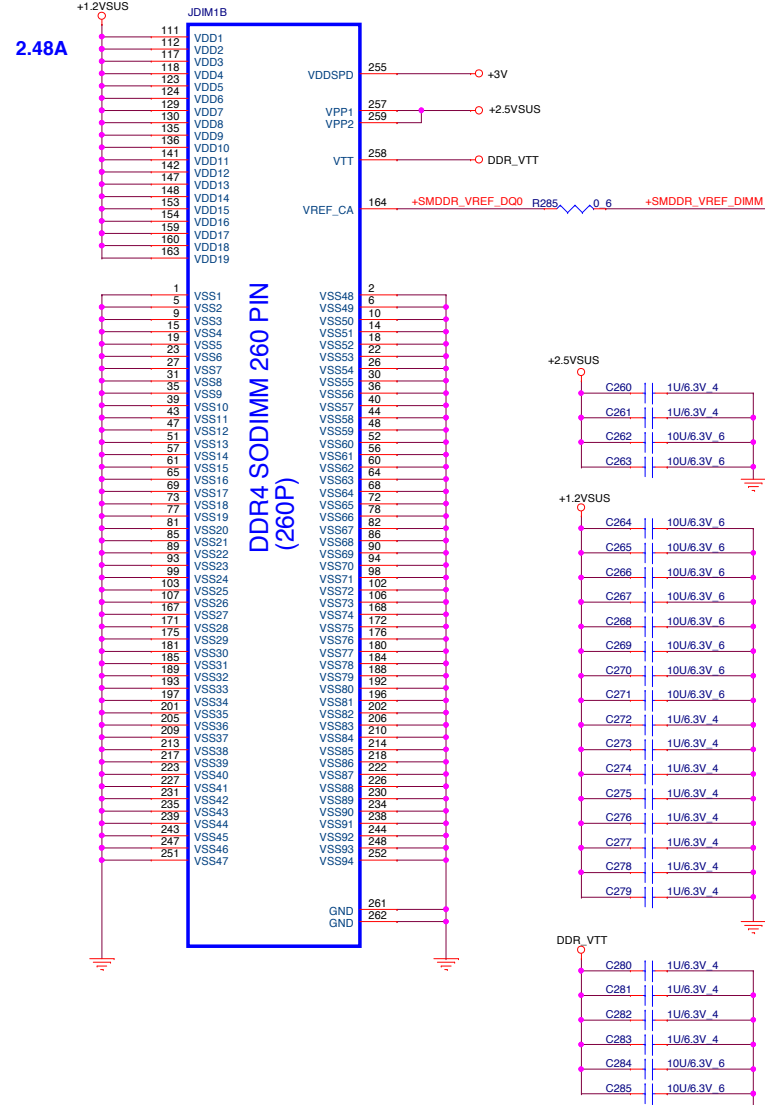
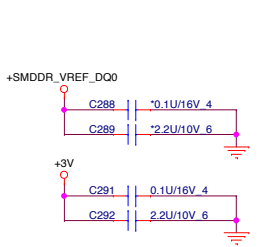
Size	Document Number	Rev
	<b>16 -- XDP &amp; APS</b>	1A
Date: Monday, December 28, 2015	Sheet 16 of 51	



+3V	5,9,10,11,12,13,14,16,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49
+2.5VSUS	18,42
+1.2VSUS	2,6,10,18,42,46,48,51
DDR_VTT	18,42



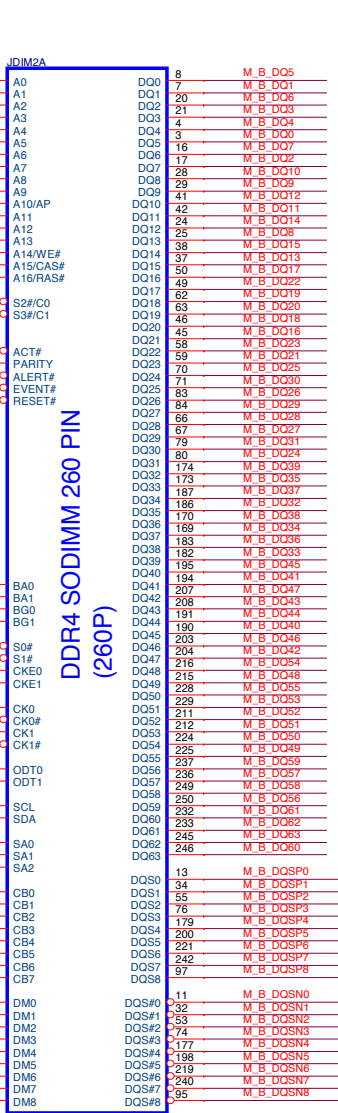
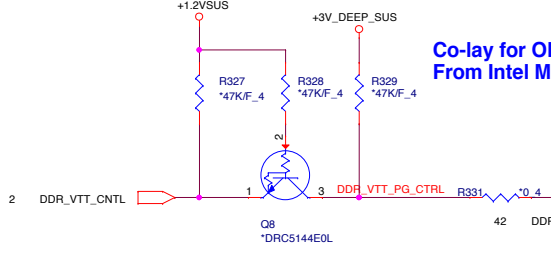
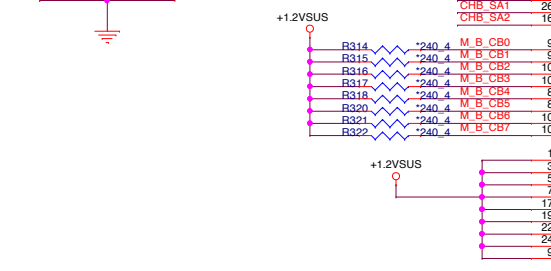
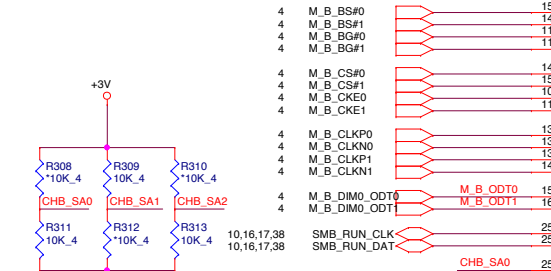
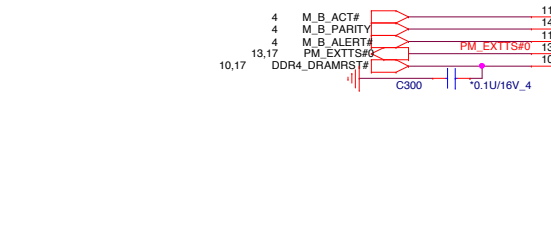
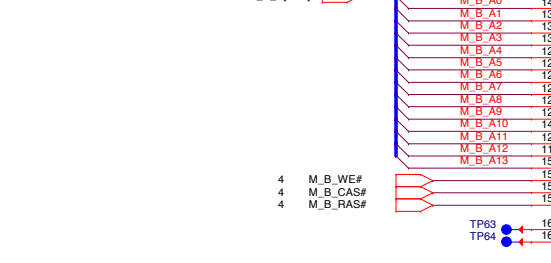
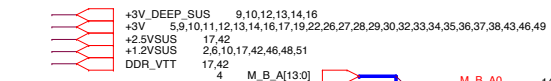
Place these Caps near So-Dimm0.



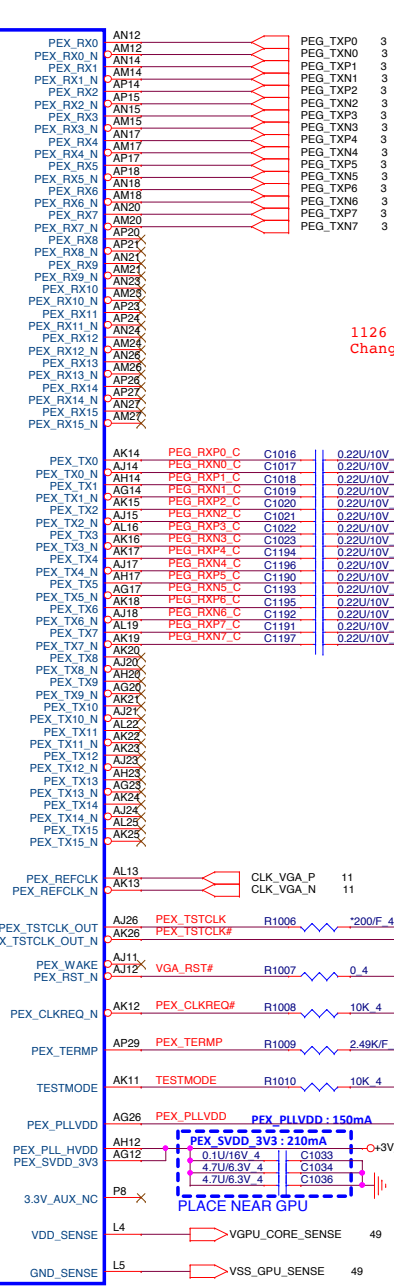
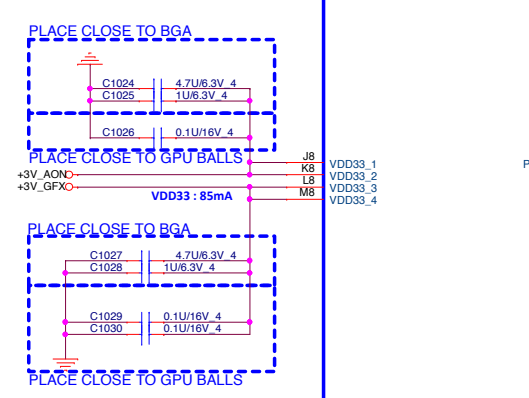
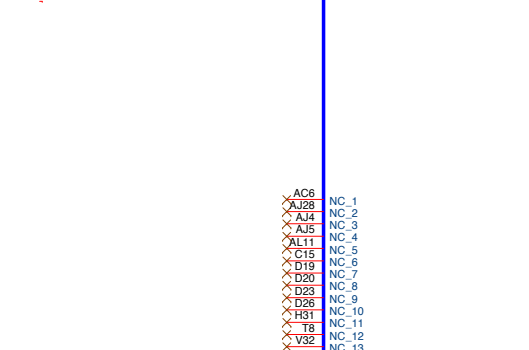
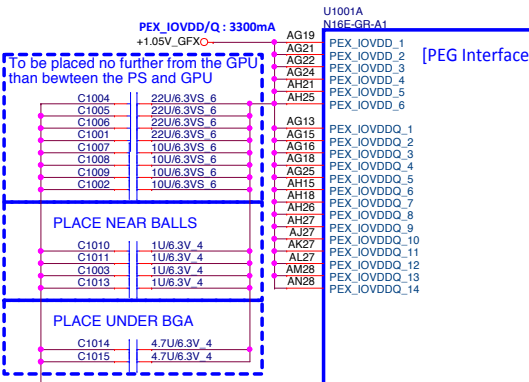
Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector

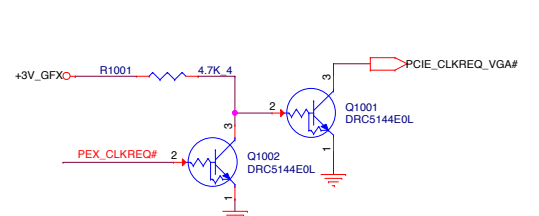
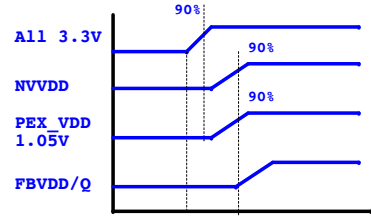
	<b>PROJECT : G37A/G37B</b>		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	17 - DDR4 DIMM0-STD(4,0H)	
Date: Monday, December 28, 2015	Sheet	17of	51



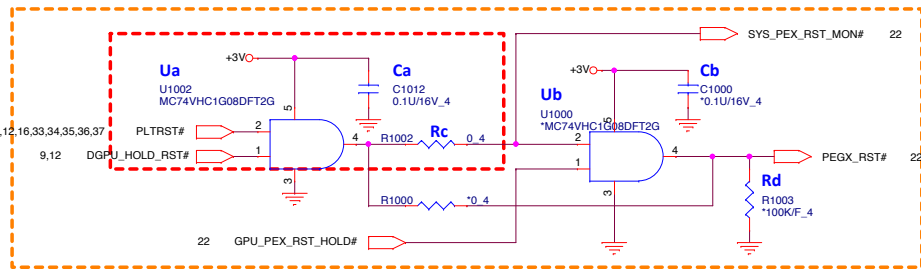
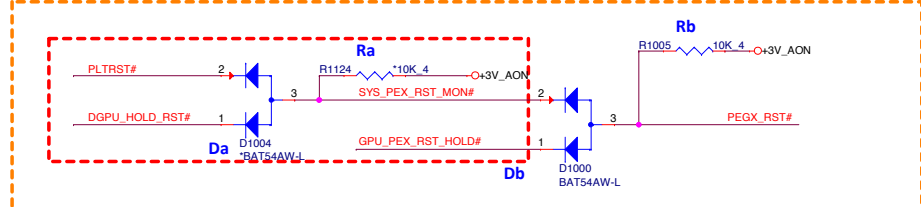
+3V 5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49  
 +3V\_AON 22,23,27,51  
 +3V\_GFX 20,21,22,23,49,51  
 +1.05V\_GFX 20,21,23,51



1126 Change D1004,R1124 from I to NI  
 Change U1002,R1002,C1012 from NI to I



If stuff Da,Db,Ra,Rb, do not stuff Ua,Ub,Ca,Cb,Rc,Rd



GPU type	Part Number	Part Description	Where Used
N16P-GT	AJ0N16P0T05	IC CTRL(908P)N16P-GT-A2(BGA)TOPBSQ	G35A
	AJ0N16P0T06	IC CTRL(908P)N16P-GT-A2(BGA)QBCON	
N16P-GX	AJ0N16P0T14	IC CTRL(908P)N16P-GX-A2(BGA)TOPBSQ	G35A / G37A
	AJ0N16P0T15	IC CTRL(908P)N16P-GX-A2(BGA)QBCON	
N16E-GR	AJ0N16E0T02	IC CTRL(908P)N16E-GR-A1(BGA)TOPBSQ	G35A / G37A
	AJ0N16E0T03	IC CTRL(908P)N16E-GR-A1(BGA)QBCON	

**PROJECT : G37A/G37B**  
 Quanta Computer Inc.

Size Custom	Document Number N16E-GR - 1/5 (PCIe)	Rev 1A
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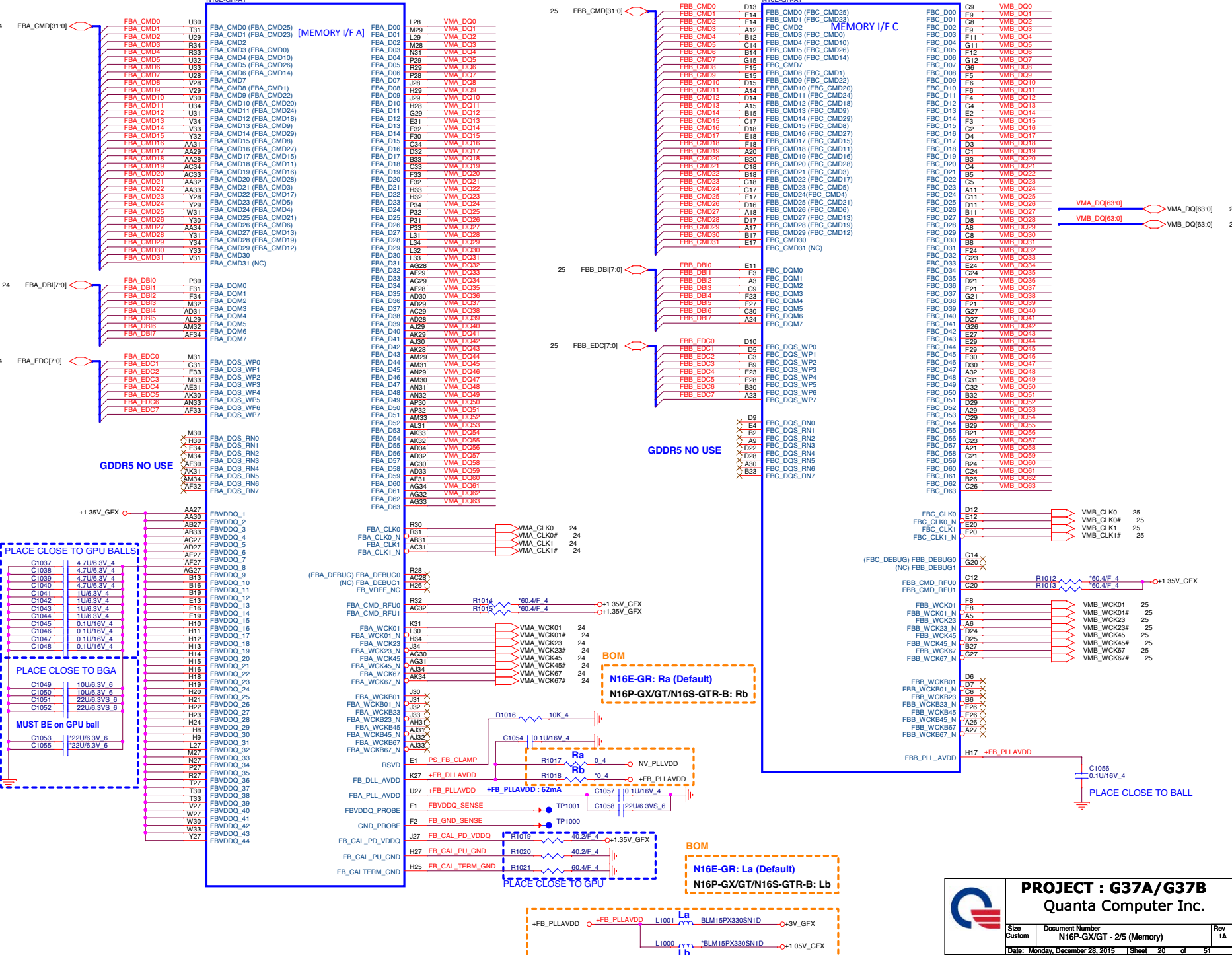
+3V\_GFX 19,21,22,23,49,51  
+1.35V\_GFX 23,24,25,50  
+1.05V\_GFX 19,21,23,51  
NV\_PLLVDD 21

U1001B  
N16E-GR-A1

U1001C  
N16E-GR-A1

[MEMORY I/F A]

[MEMORY I/F C]



PLACE CLOSE TO GPU BALLS

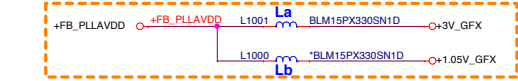
PLACE CLOSE TO BGA

MUST BE on GPU ball

GDDR5 NO USE

BOM  
N16E-GR: Ra (Default)  
N16P-GX/GT/N16S-GTR-B: Rb

BOM  
N16E-GR: La (Default)  
N16P-GX/GT/N16S-GTR-B: Lb



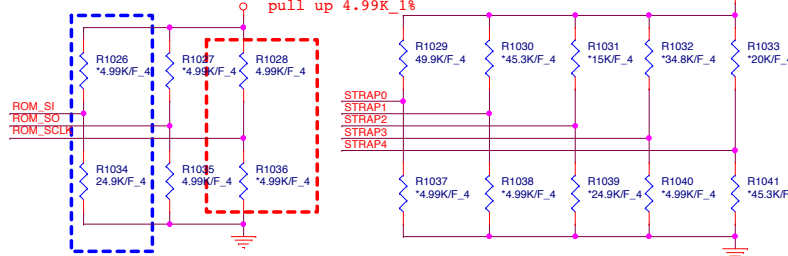
PROJECT : G37A/G37B  
Quanta Computer Inc.  
Size Custom Document Number N16P-GX/GT - 2/5 (Memory) Rev 1A  
Date: Monday, December 28, 2015 Sheet 20 of 51



+3V 5,9,10,11,12,13,14,16,17,18,19,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49  
 +3V\_AON 19,23,27,51  
 +3V\_GFX 19,20,21,23,49,51

Default: MicronVRAM 4GB

1130 Mount R1028 4.99K GPU HDMI output from GPU IPPE, ROM\_SCLK= 1000 => pull up 4.99K 1%



GPU Netname	N16P-GT	N16P-GX	N16E-GR
ROM_SO	4.99K PD	4.99K PD	4.99K PD
ROM_SCLK	4.99K PU	4.99K PU	4.99K PU
STRAP0	49.9K PU	49.9K PU	49.9K PU
STRAP1	NC	NC	NC
STRAP2	NC	NC	NC
STRAP3	NC	NC	NC
STRAP4	NC	NC	NC

4.99K/F\_4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)  
 10K/F\_4: CS31002FB26 RES CHIP 10K 1/16W +1%(0402)  
 15K/F\_4: CS31502FB24 RES CHIP 15K 1/16W +1%(0402)  
 20K/F\_4: CS32002FB29 RES CHIP 20K 1/16W +1%(0402)  
 24.9K/F\_4: CS32492FB16 RES CHIP 24.9K 1/16W +1%(0402)  
 30.1K/F\_4: CS33012FB18 RES CHIP 30.1K 1/16W +1%(0402)  
 34.8K/F\_4: CS33482FB22 RES CHIP 34.8K 1/16W +1%(0402)  
 45.3K/F\_4: CS34532FB18 RES CHIP 45.3K 1/16W +1%(0402)

VRAM Table of N16P-GT N16P-GT device ID = 0x139A

Vendor	TOP B/S QBCON	Mfr. P/N	SIZE	ROM_SI
Hynix	AKG5PWUTW19	H5GC4H24AJR-T2C	256Mx16	0x6 0110 PD 34.8K
	AKG5PWUTW20			0x4 0100 PD 24.9K
Micron	AKG5PW0TL05	EDW4032BABG-60-F-D	256Mx32	0x8 1001 PU 10K
	AKG5PW0TL06			0x3 0011 PD 20K

Resistor Values	PU to 3V3_MAIN	PD to GND
4.99K OHM	1000	0000
10K OHM	1001	0001
15K OHM	1010	0010
20K OHM	1011	0011
24.9K OHM	1100	0100
30.1K OHM	1101	0101
34.8K OHM	1110	0110
45.3K OHM	1111	0111

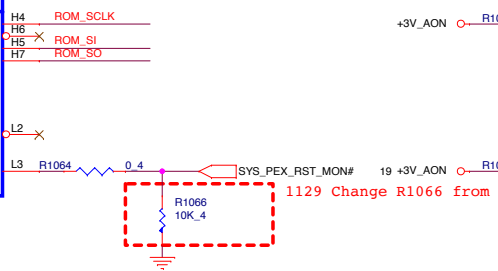
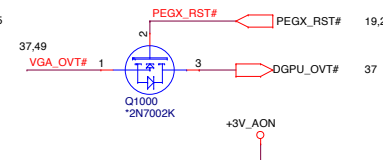
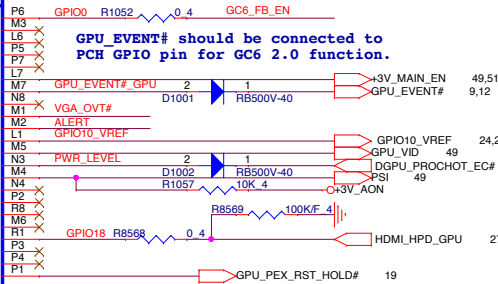
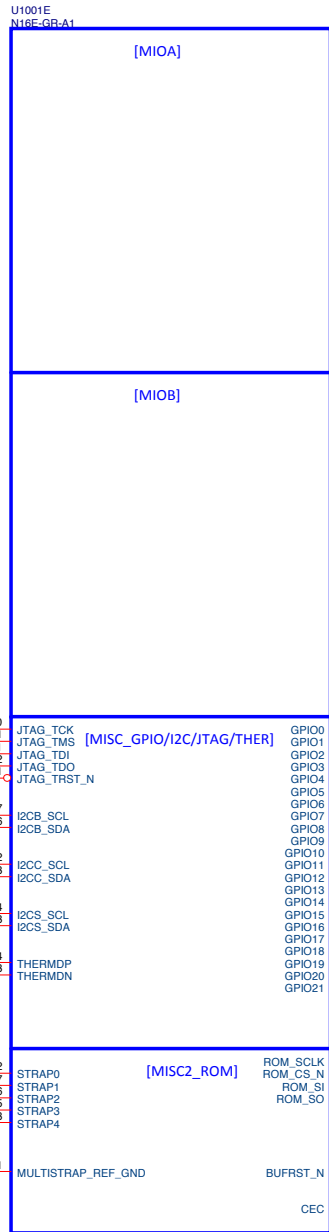
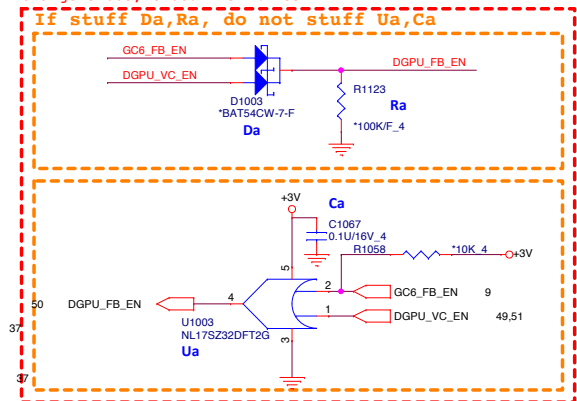
VRAM Table of N16P-GX N16P-GX device ID = 0x139B

Vendor	TOP B/S QBCON	Mfr. P/N	SIZE	ROM_SI
Hynix	AKG5PWUTW19	H5GC4H24AJR-T2C	256Mx16	0x6 0110 PD 34.8K
	AKG5PW0TL05			0x4 0100 PD 24.9K
Micron	AKG5PW0TL06	EDW4032BABG-60-F-D	256Mx32	0x9 1001 PU 10K
	AKG5LGUTL02			0x8 1000 PU 4.99K
Samsung	AKG5QGDT503	K4G80325FB-HC03	256Mx32	0x8 1000 PU 4.99K
	AKG5QGDT504			0x8 1000 PU 4.99K

VRAM Table of N16E-GR N16E-GR device ID = 0x1427

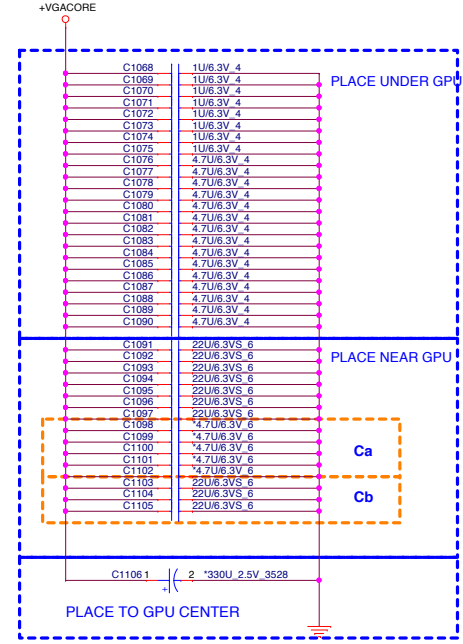
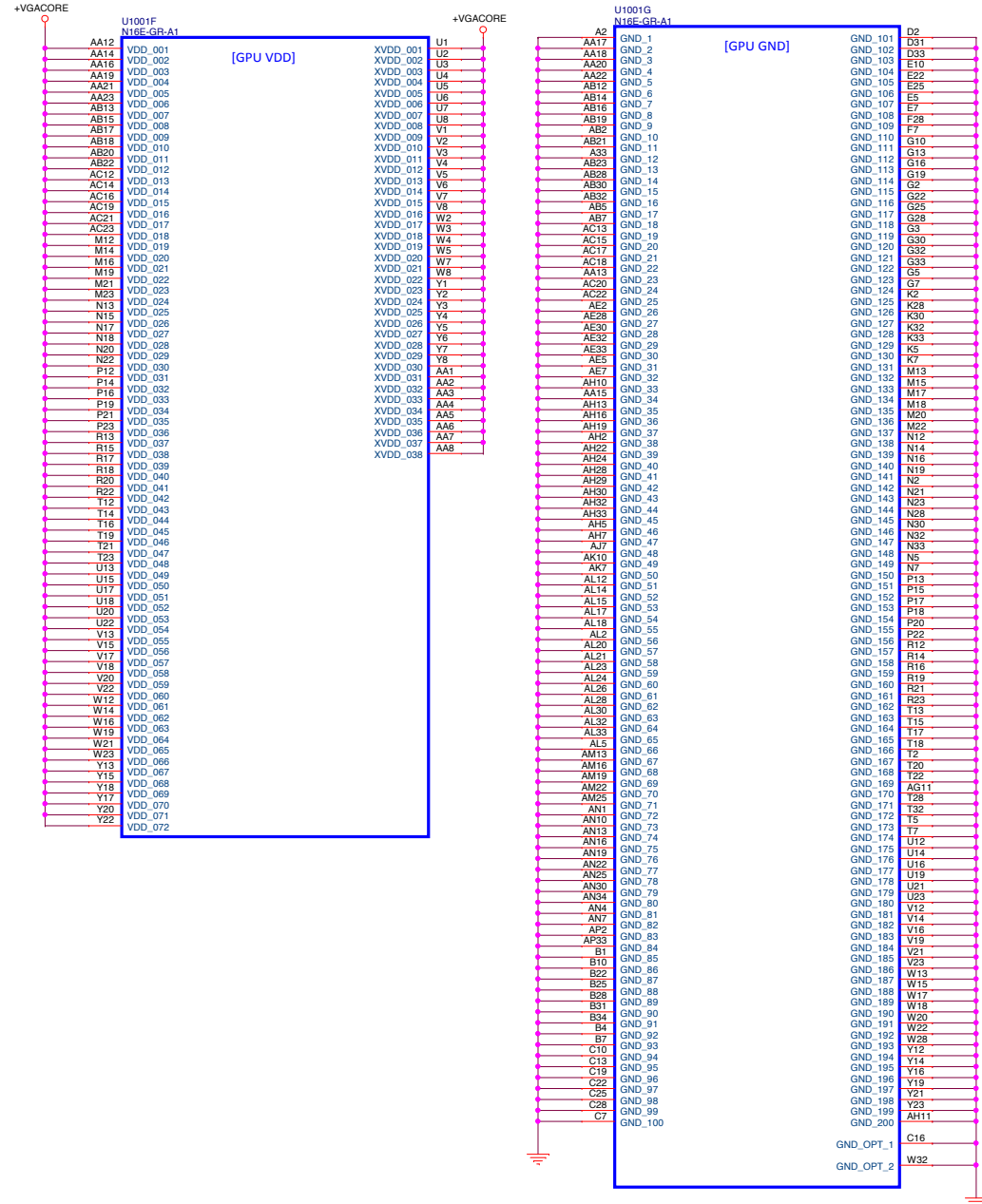
Vendor	TOP B/S QBCON	Mfr. P/N	SIZE	ROM_SI
Hynix	AKG5PWUTW19	H5GC4H24AJR-T2C	256Mx16	0x0 0000 PD 4.99K
	AKG5PWUTW20			0x4 0100 PD 24.9K
Micron	AKG5PW0TL05	EDW4032BABG-60-F-D	256Mx32	0x8 1001 PU 10K
	AKG5LGUTL02			0x4 0100 PD 24.9K
Samsung	AKG5QGDT503	K4G80325FB-HC03	256Mx32	0x3 0011 PD 20K
	AKG5QGDT504			0x3 0011 PD 20K

1126 Change D1003, R1123 from I to NI  
 Change U1003, C1067 from NI to I  
 If stuff Da, Ra, do not stuff Ua,Ca



+3V_AON	19,22,27,51
+3V_GFX	19,20,21,22,49,51
+1.35V_GFX	20,24,25,50
+1.05V_GFX	19,20,21,51
+VGACORE	49

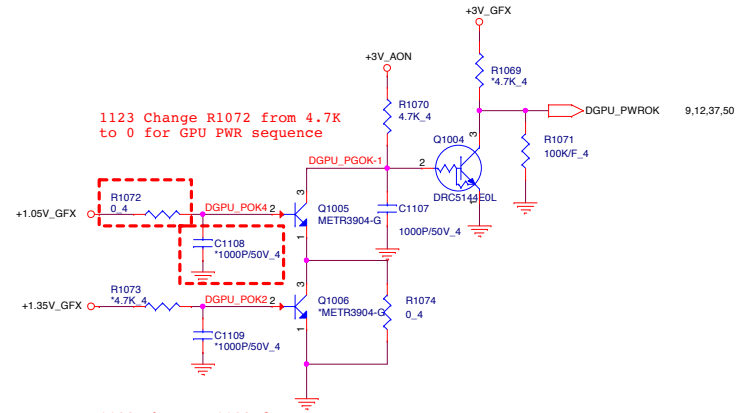
## VDD/XVDD : 62A



**GPU BOM:**  
 N16E-GR: Ca Unstuff, Cb Stuff (Default)  
 N16P-GX/GT/N16S-GTR-B: Ca change 4.7u stuff, Cb unstuff

4.7 uF : CH5471K9E07 CAP CHIP  
 4.7U 6.3V(+10%,X5R,0603)

### For meet Power down sequence for +3V\_GFX



**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

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CHANNEL A: 2G/4G GDDR5

+1.35V\_GFX 20,23,25,50

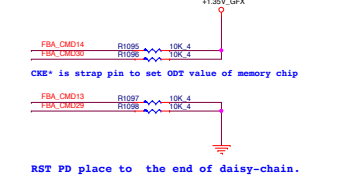
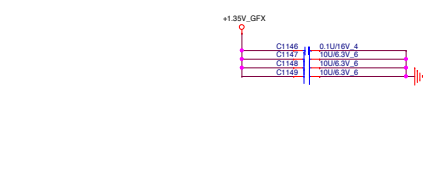
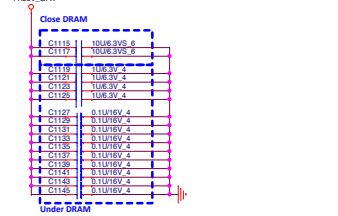
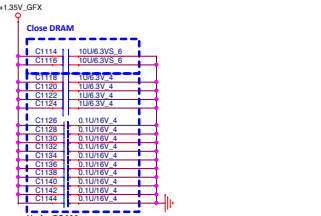
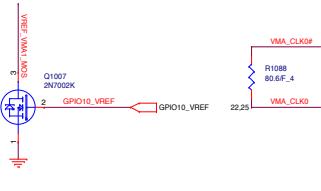
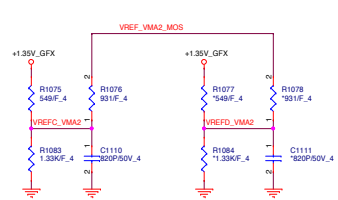
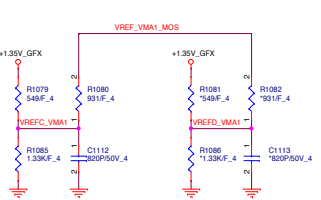
MF=0 Non-mirrored

MF=0 Non-mirrored



- QD24-31
- QD16-23
- QD8-15
- QD0-7

- QD56-63
- QD48-55
- QD40-47
- QD32-39



**GDDR5 Mode H Mapping**

< 0-31 > < 32-63 > Memory

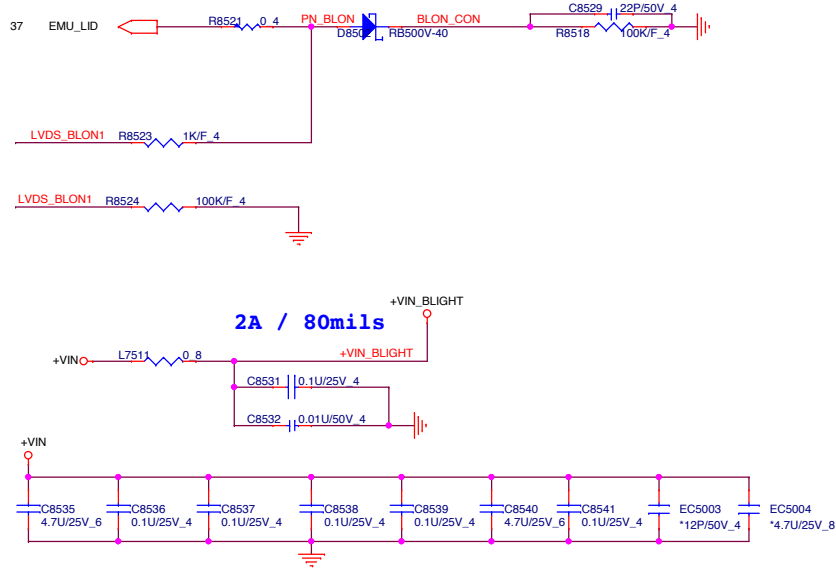
CHD0	CHD16	CS*
CHD1	CHD17	A3_BA3
CHD2	CHD18	A2_BA0
CHD3	CHD19	A4_BA2
CHD4	CHD20	A5_BA1
CHD5	CHD21	WE*
CHD6	CHD22	A7_A8
CHD7	CHD23	A6_A11
CHD8	CHD24	AB1*
CHD9	CHD25	A12_RFU
CHD10	CHD26	A0_A10
CHD11	CHD27	A1_A9
CHD12	CHD28	RAS*
CHD13	CHD29	RST*
CHD14	CHD30	CKE*
CHD15	CHD31	CAS*



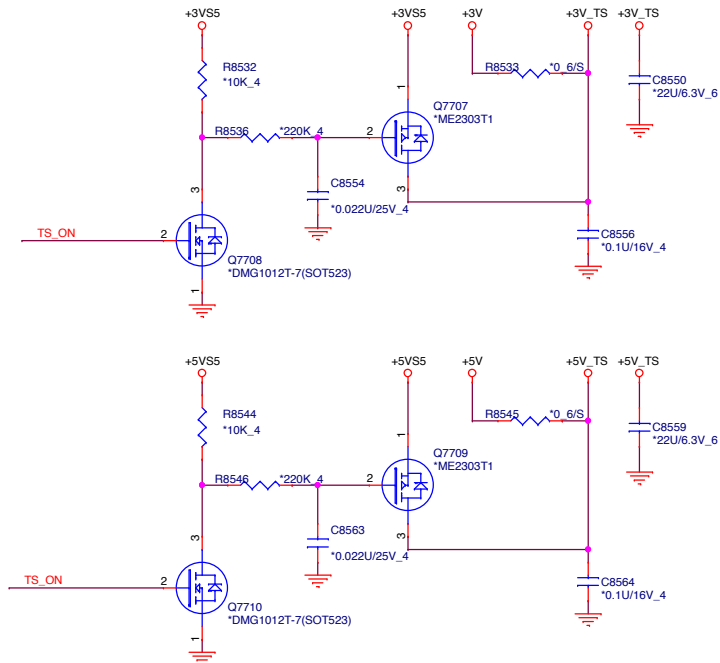


+VIN	32,38,39,40,41,42,43,44,45,47,48,49,50
+5VS5	10,28,30,41,42,43,44,45,46,47,48,49,50,51
+5V	27,28,29,31,32,38,46,49
+3VS5	10,12,14,16,33,37,41,42,46,47,48,51
+3V	5,9,10,11,12,13,14,16,17,18,19,22,27,28,29,30,32,33,34,35,36,37,38,43,46,49
+3V_CAM	34

# LID Switch



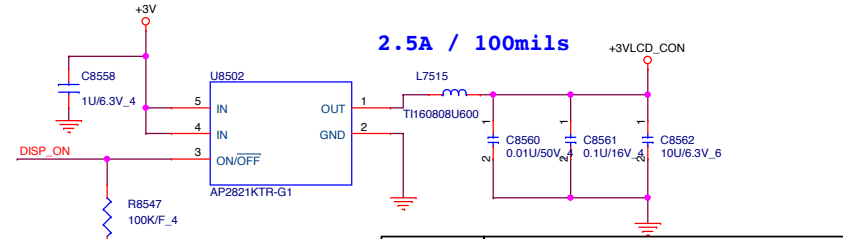
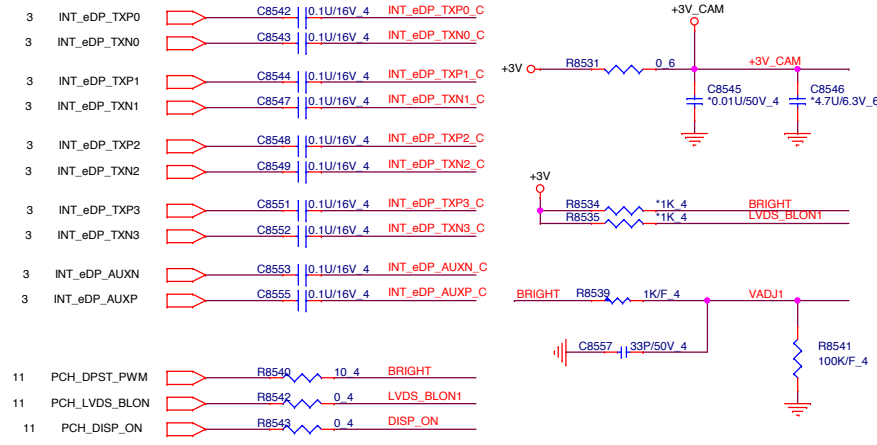
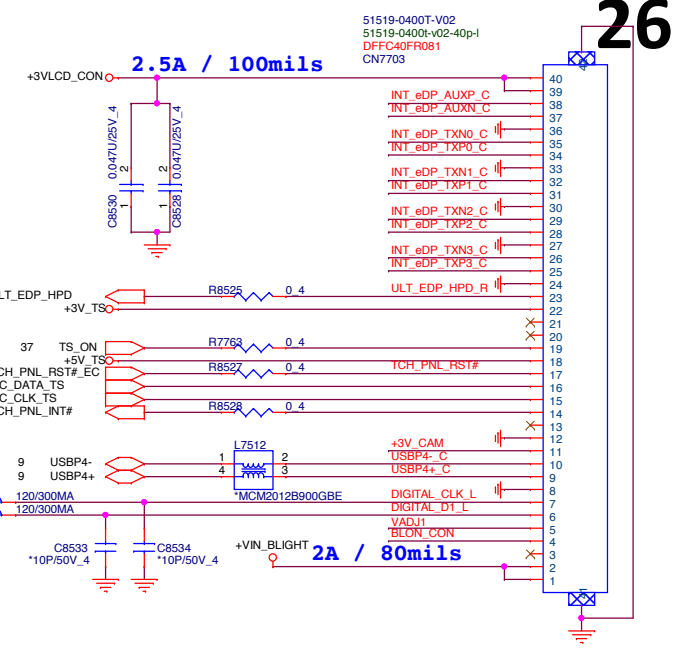
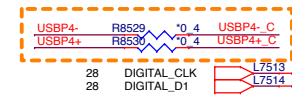
# Touch screen



# eDP Conn.

MB	TS (V/F: I2C)
+3V_TS	VDD33
I2C_DATA_TS	SDA
I2C_CLK_TS	SCL
TCH_PNL_RST#_EC	EXRESETN
TCH_PNL_INT#	ATTN
TS_ON	Report_Switch
GND	GND

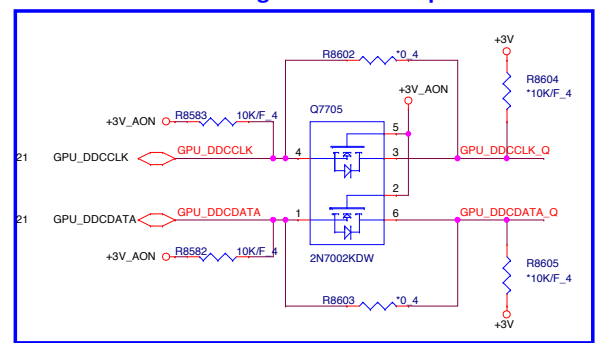
BOM: HD CAM Stuff  
BOM: 3D CAM Un-Stuff



**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

Size Custom	Document Number	Rev
	<b>26 -- LCD CONN/LID/CAM/D-MIC/TS1A</b>	
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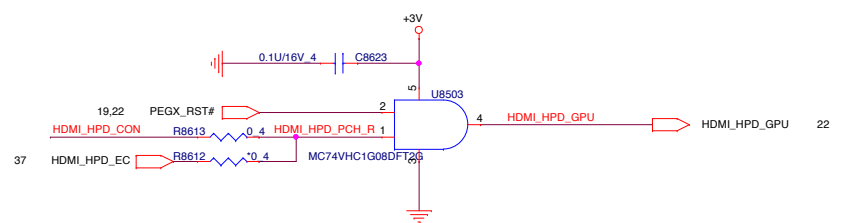
### Prevent current leakage when GPU is power off



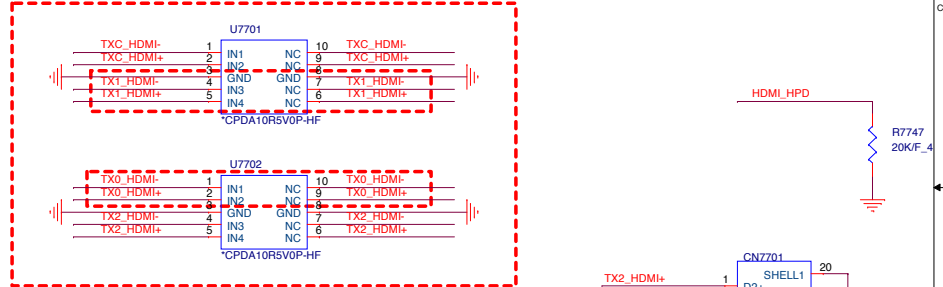
### EMI Solution



1127 Change P/N from CH+7506XB02 to CH+7506TB01

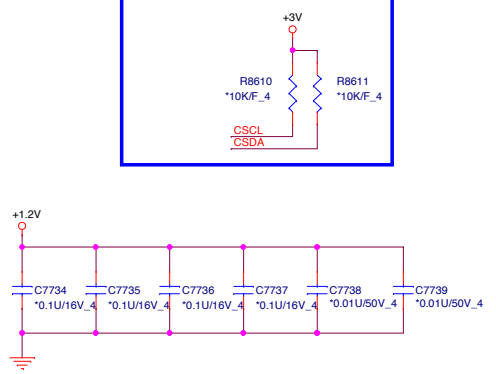


### ESD

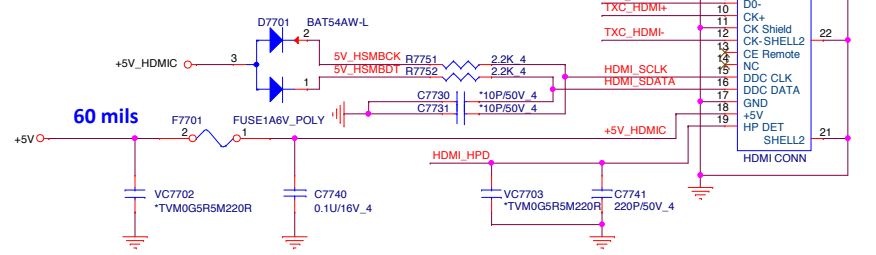
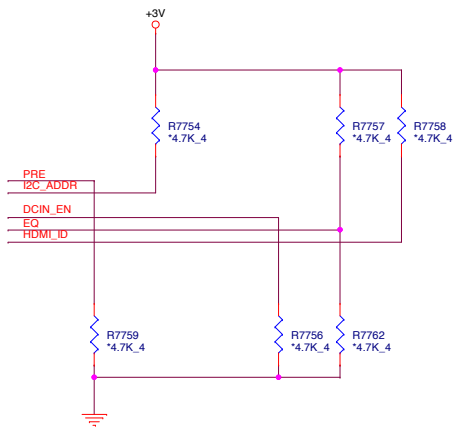
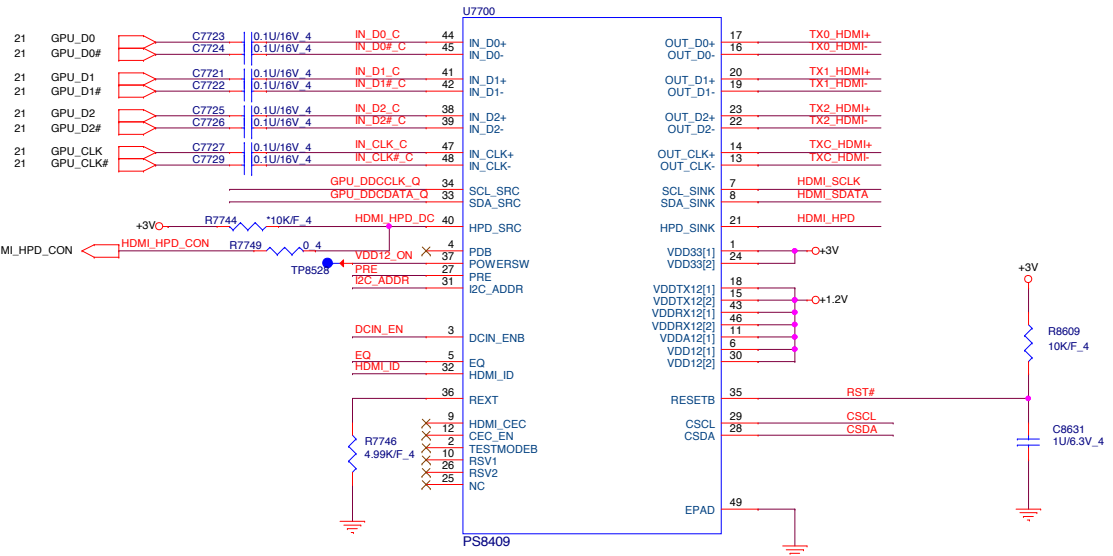


1124 Reserve ESD protection component  
1124 SWAP for Layout

### Optional

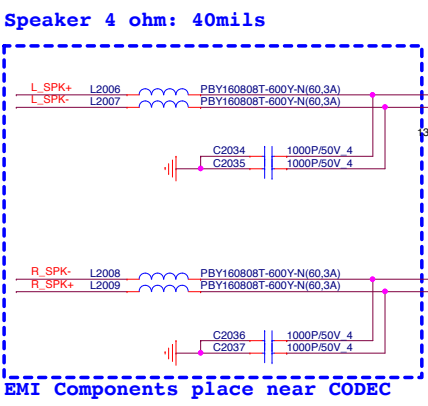
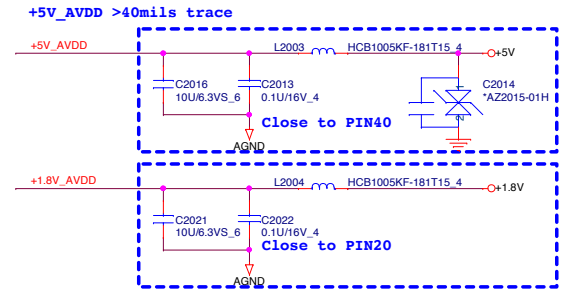
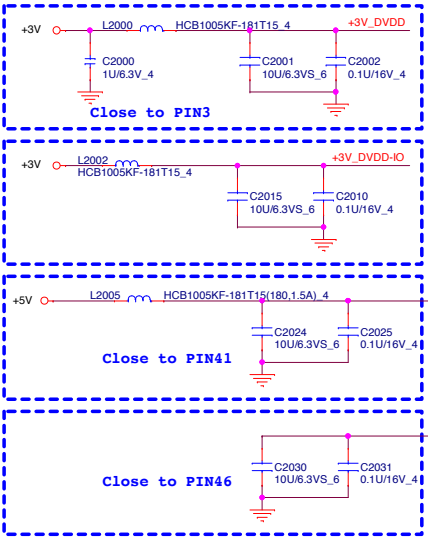


+5V	26,28,29,31,32,38,46,49
+3V	5,9,10,11,12,13,14,16,17,18,19,22,26,28,29,30,32,33,34,35,36,37,38,43,46,49
+1.2V	46

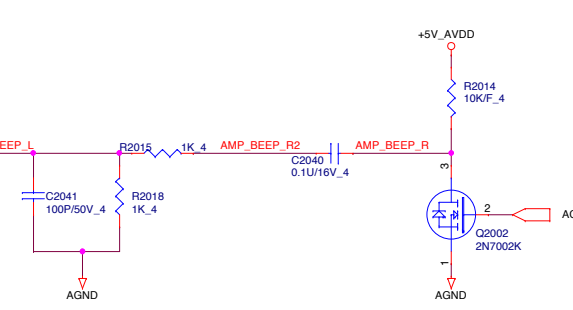
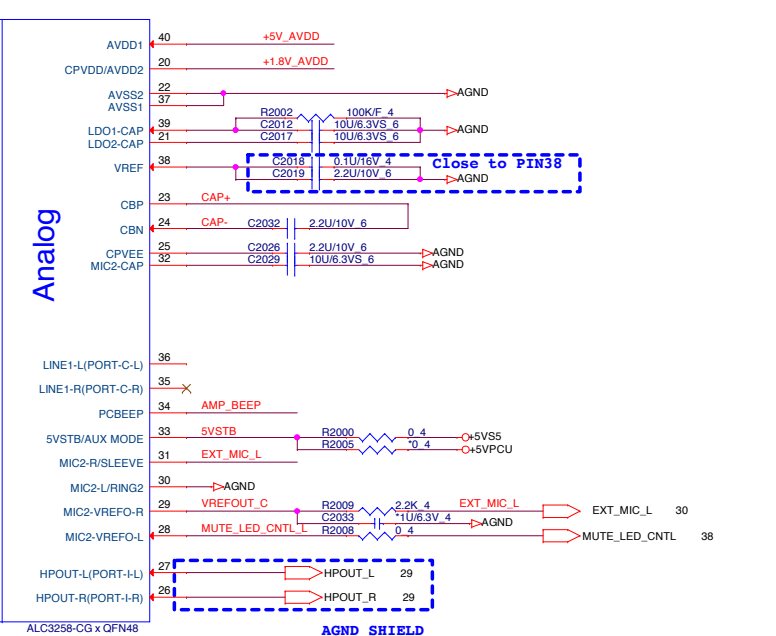
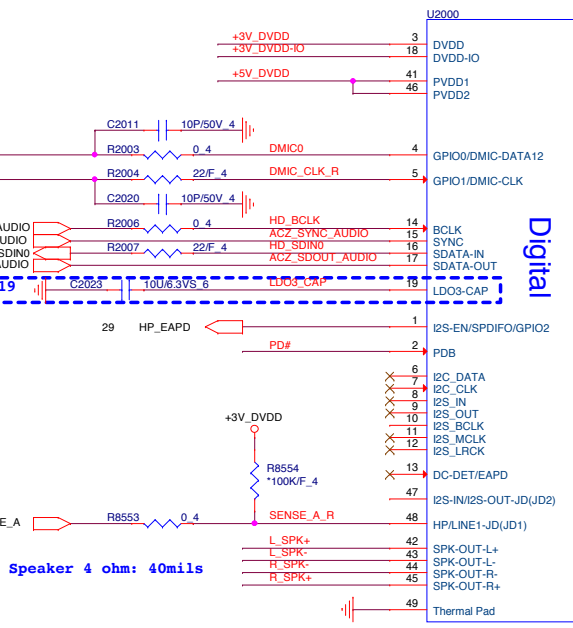
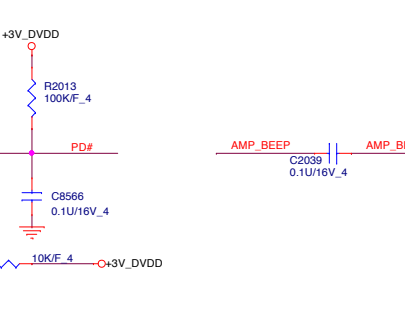
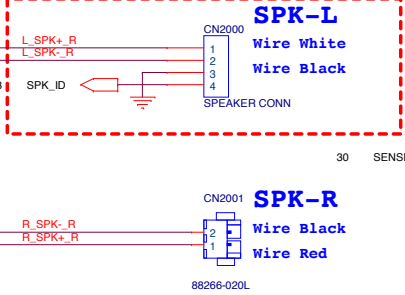


<b>PROJECT : G37A/G37B</b>		
<b>Quanta Computer Inc.</b>		
Size Custom	Document Number <b>27 -- HDMI/HDMI REDRIVER</b>	Rev 1A
Date: Monday, December 28, 2015	Sheet 27 of	51

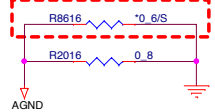
+5V	26,27,29,31,32,38,46,49
+3V	5,9,10,11,12,13,14,16,17,18,19,22,26,27,29,30,32,33,34,35,36,37,38,43,46,49
+1.8V	31,47



1123 Change CN2000 P/N and FP 2Pin to 4Pin for SPK Vendor ID used



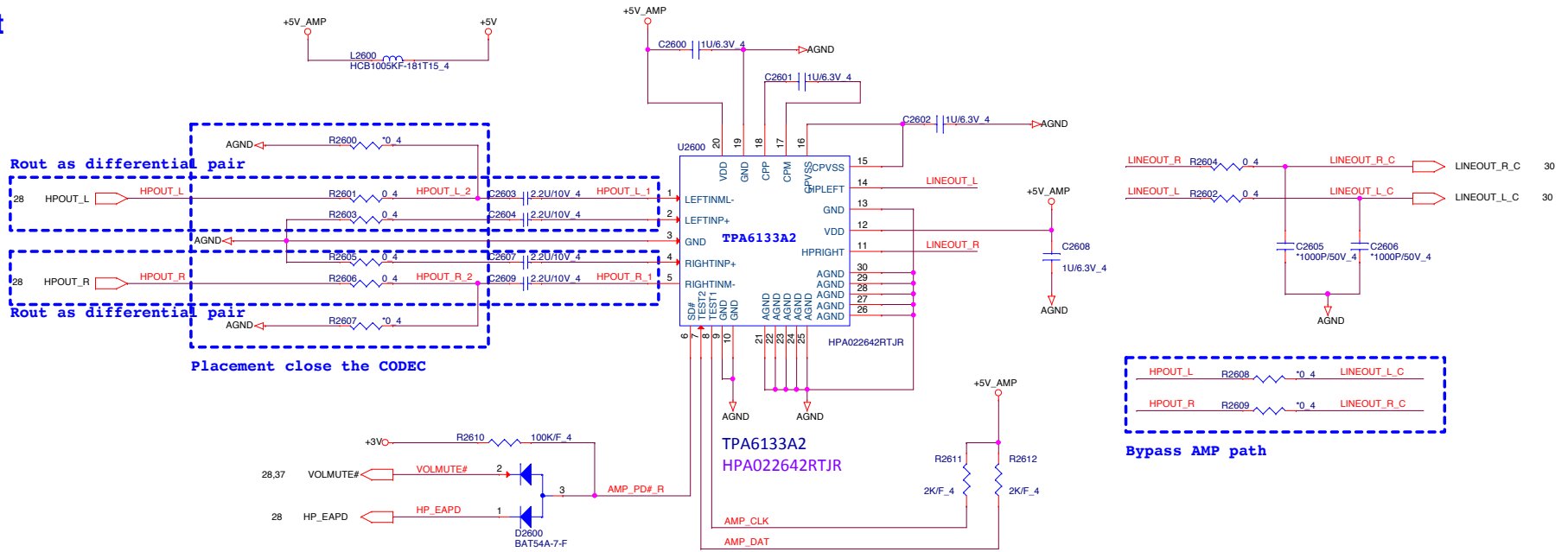
place to near or under codec  
1125 Add R8616 0603size short pad under codec for EMI request




		<b>PROJECT : G37A/G37B</b> Quanta Computer Inc.	
Date: Monday, December 28, 2015		Sheet 26	of 51

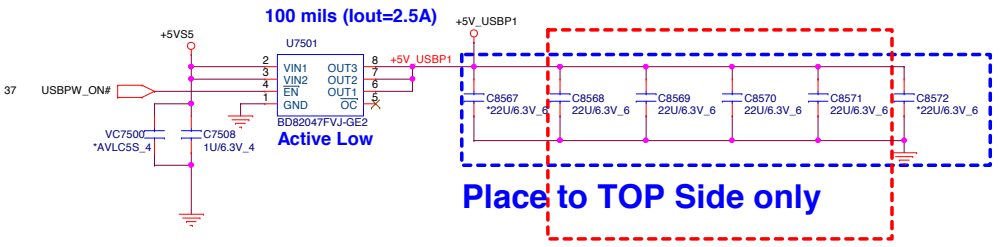
# Head Phone out

+5V 26,27,28,31,32,38,46,49  
 +3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,30,32,33,34,35,36,37,38,43,46,49



	<b>PROJECT : G37A/G37B</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number <b>29-- HP AMP HPA022642RTJR</b>	Rev 1A
Date: Monday, December 28, 2015   Sheet 29 of 51			

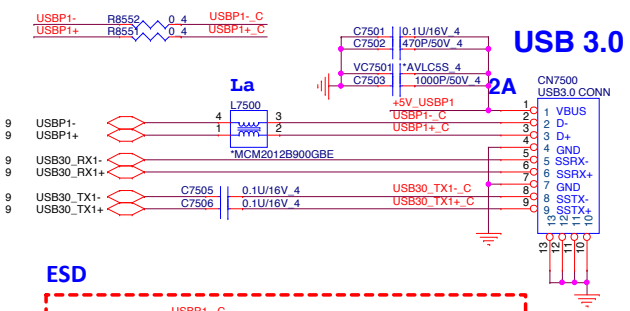
+5VSS	10,26,28,41,42,43,44,45,46,47,48,49,50,51
+3VPCU	5,10,33,37,38,40,41
+3V	5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,32,33,34,35,36,37,38,43,46,49
+1.8V	28,31,47



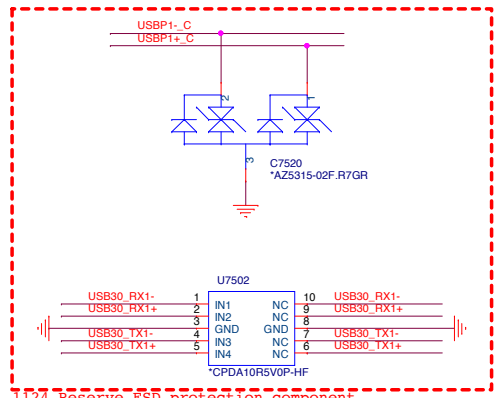
Place to TOP Side only

1125 Mount C8568,C8569,C8570,C8571 for SVTP USB ports Short Test

### USB 2.0/3.0 Combo

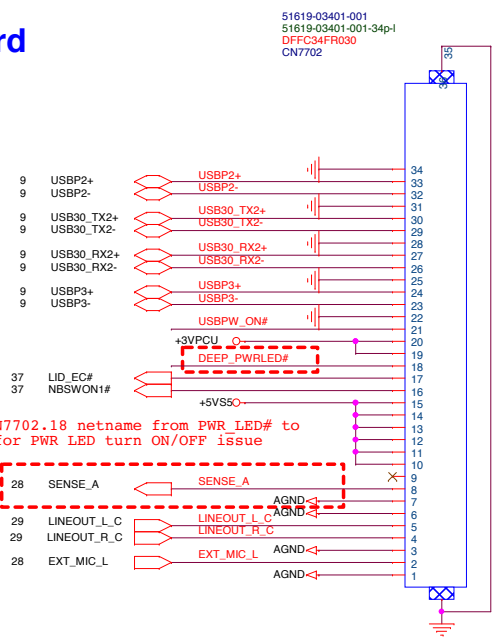


### ESD



1124 Reserve ESD protection component

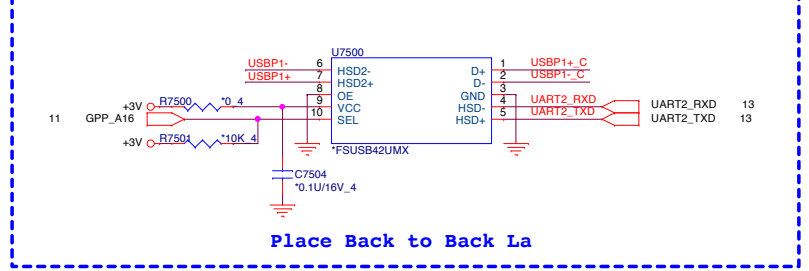
### Daughter Board



1123 Change CN7702.18 netname from PWR\_LED# to DEEP\_PWRLED# for PWR LED turn ON/OFF issue

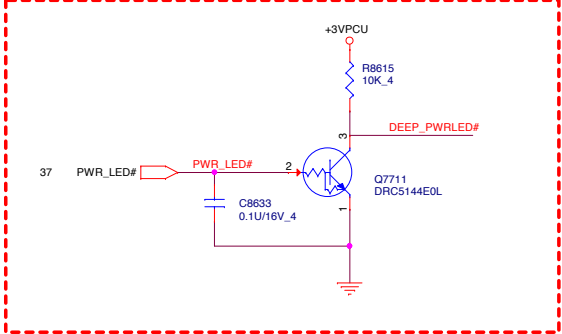
1124 Pin7 and Pin8 need SWAP due to SENSE\_A is refer to DGND so

### UART for Win7 WHQL DEBUG



Place Back to Back La

### 1123 Add PWR LED MOS Circuit

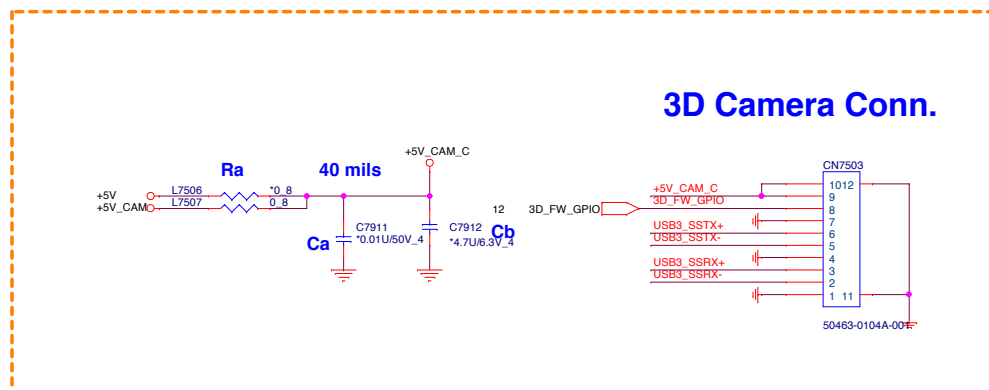


**PROJECT : G37A/G37B**  
Quanta Computer Inc.

Size Custom	Document Number <b>30 - USB3.0/DB</b>	Rev 1A
Date: Monday, December 28, 2015   Sheet 30 of 51		

+5V	26,27,28,29,32,38,46,49
+3VPCU	5,10,30,33,37,38,40,41
+3V	5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49
+1.8V	28,47

BOM: 3D Cam Stuff (except Ra,Ca,Cb)  
 BOM: HD CAM Un- Stuff



BOM: 3D Cam Stuff (except Rb, Rc)

BOM: HD CAM Un-Stuff

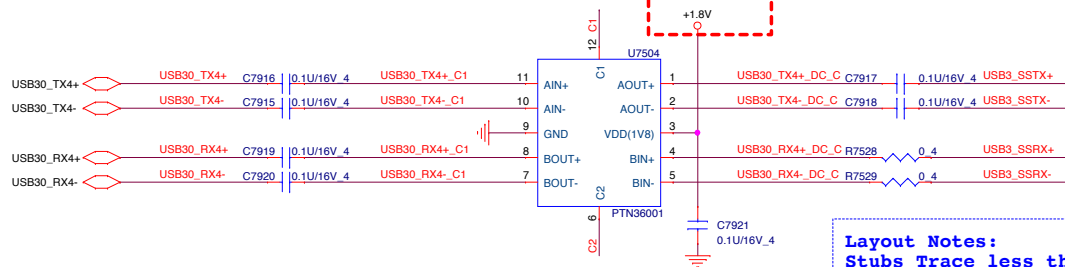
## USB3.0

### USB3.0 Re-driver IC

HOST

USB3.0 re-driver IC

DEVICE



Layout Notes:  
 Stubs Trace less than 150mil

1123 Change UB3 re driver power rail from +1.8V\_DEEP\_SUS to +1.8V

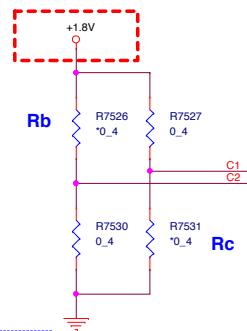


Table 4. C1 pin controls long/medium/short traces

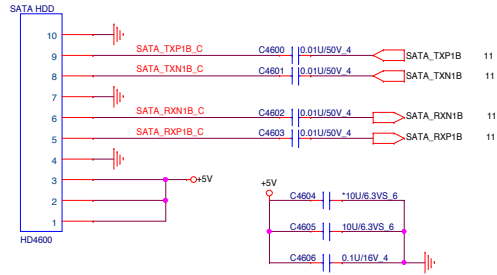
State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ <sup>[1]</sup>	DE <sup>[2]</sup>	OS <sup>[3]</sup>
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Table 5. C2 pin controls long/medium/short traces

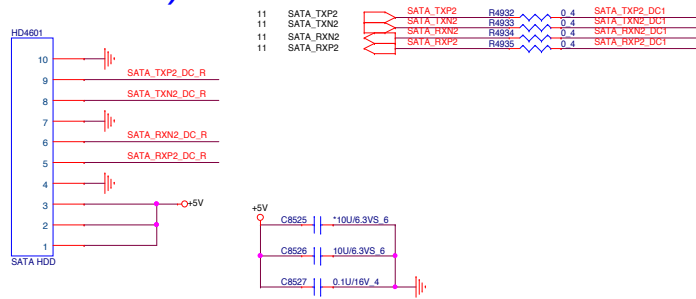
State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ <sup>[1]</sup>	DE <sup>[2]</sup>	OS <sup>[3]</sup>
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

+VIN 26,38,39,40,41,42,43,44,45,47,48,49,50  
 +5V 26,27,28,29,31,38,46,49  
 +3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,33,34,35,36,37,38,43,46,49

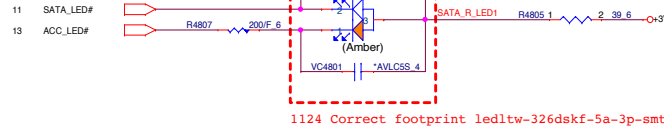
**HDD**



**HDD (Close to ODD)**

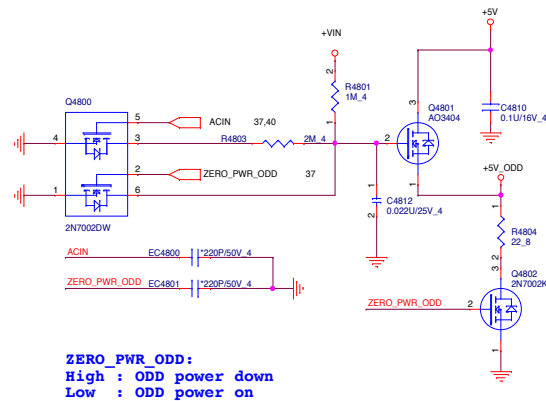
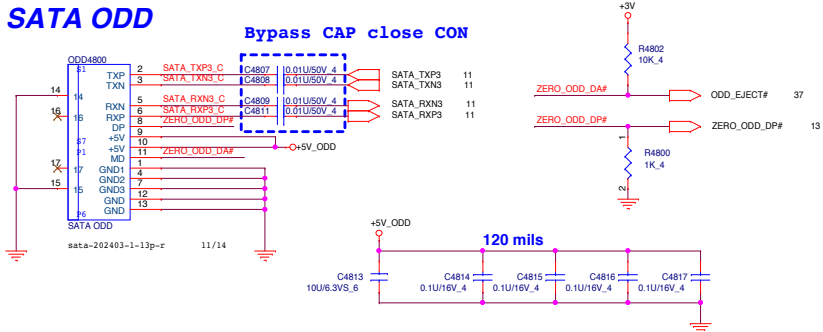


**SATA LED**



SATA_TXP2_DC1	C4924	0.01U/50V_4	SATA_TXP2_DC_R
*SATA_TXN2_DC1	C4925	0.01U/50V_4	*SATA_TXN2_DC_R
*SATA_RXN2_DC1	C4926	0.01U/50V_4	*SATA_RXN2_DC_R
*SATA_RXP2_DC1	C4927	0.01U/50V_4	*SATA_RXP2_DC_R

**SATA ODD**

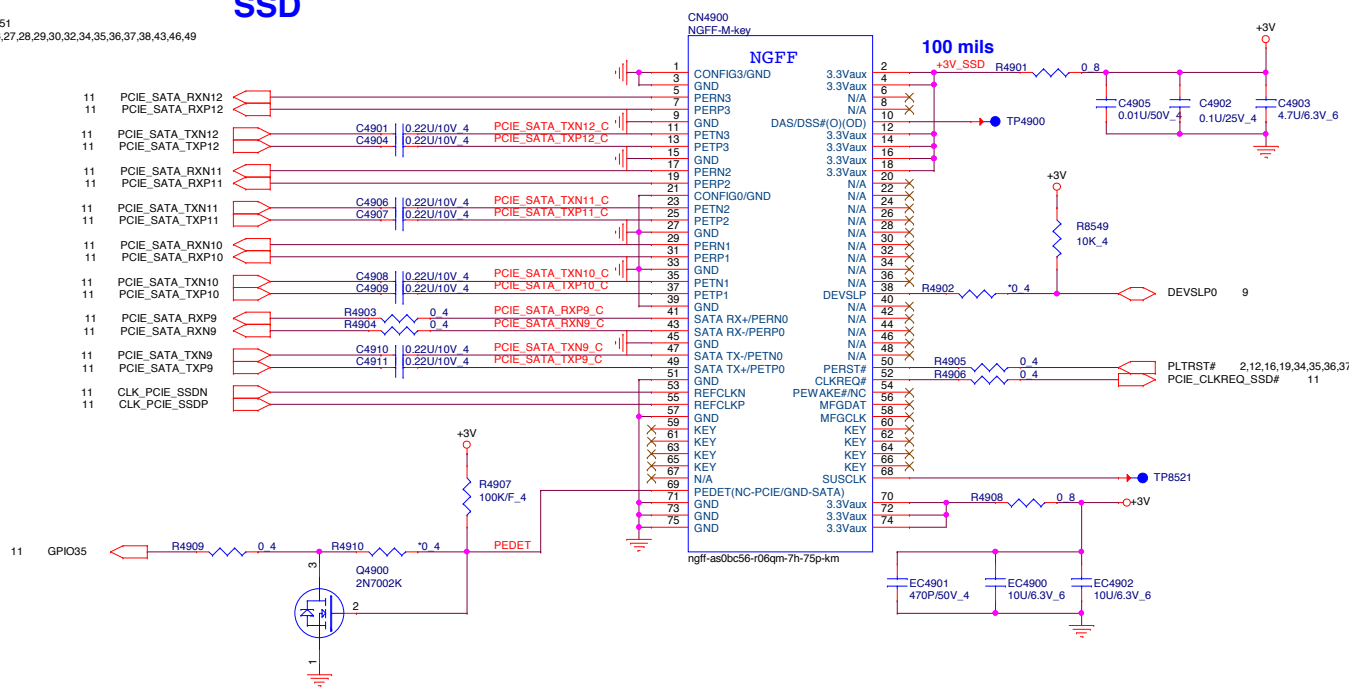


**ZERO\_PWR\_ODD:**  
 High : ODD power down  
 Low : ODD power on

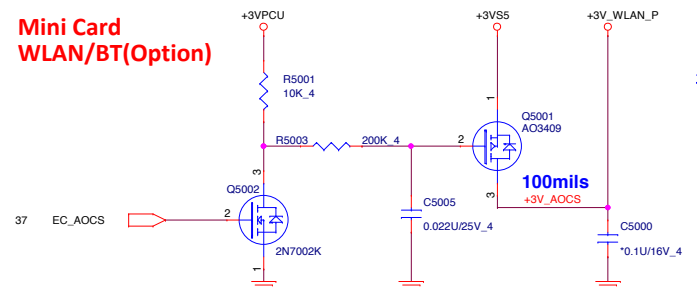


# SSD

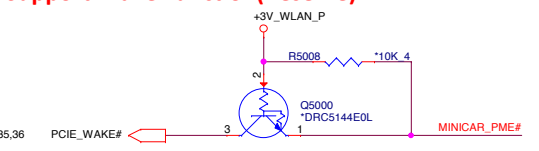
+3VPCU 5,10,30,37,38,40,41  
 +3VSS 10,12,14,16,26,37,41,42,46,47,48,51  
 +3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,34,35,36,37,38,43,46,49



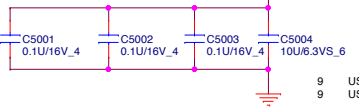
## Mini Card WLAN/BT(Optional)



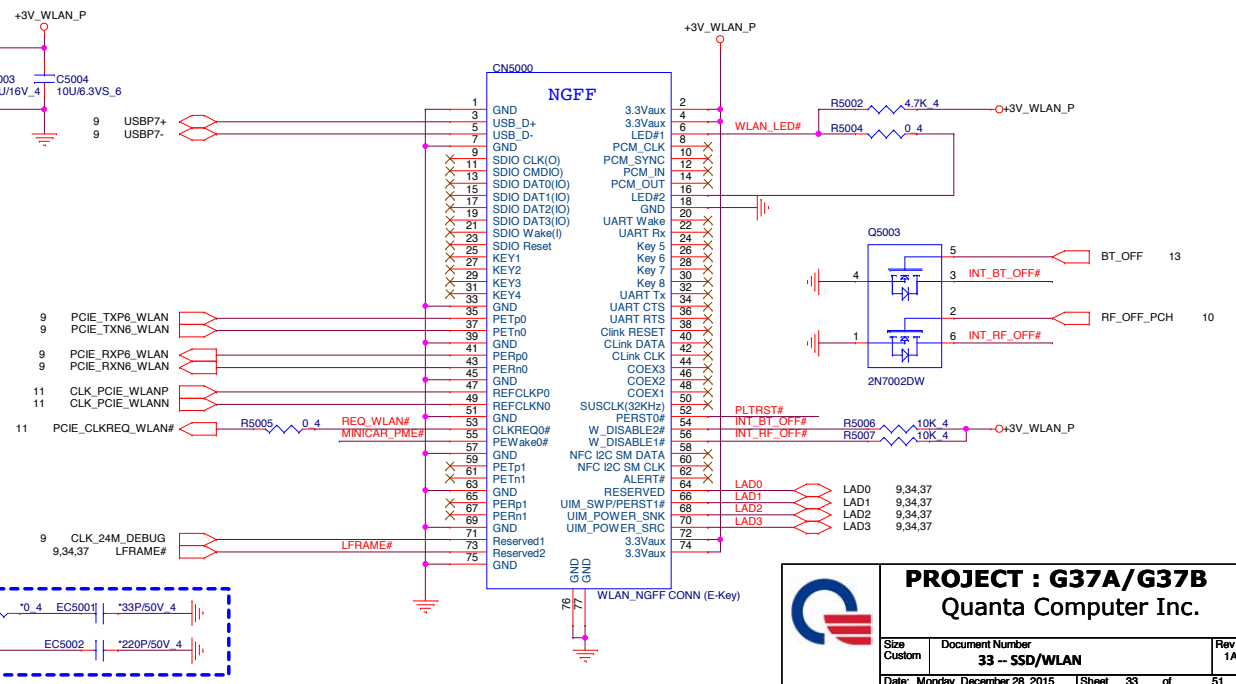
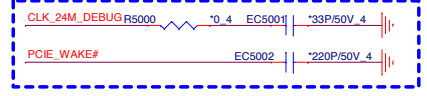
## Support Wake Function(Reserve)



## 100 mils



### For EMI Suggestion

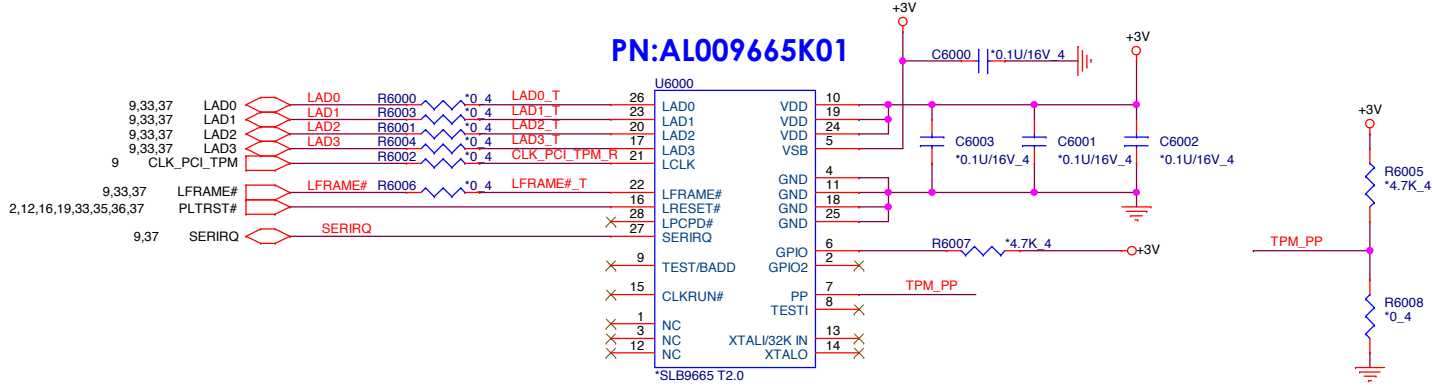


**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>33 -- SSD/WLAN</b>	Rev <b>1A</b>
Date: Monday, December 28, 2015   Sheet 33 of 51		

# TPM (2.0)

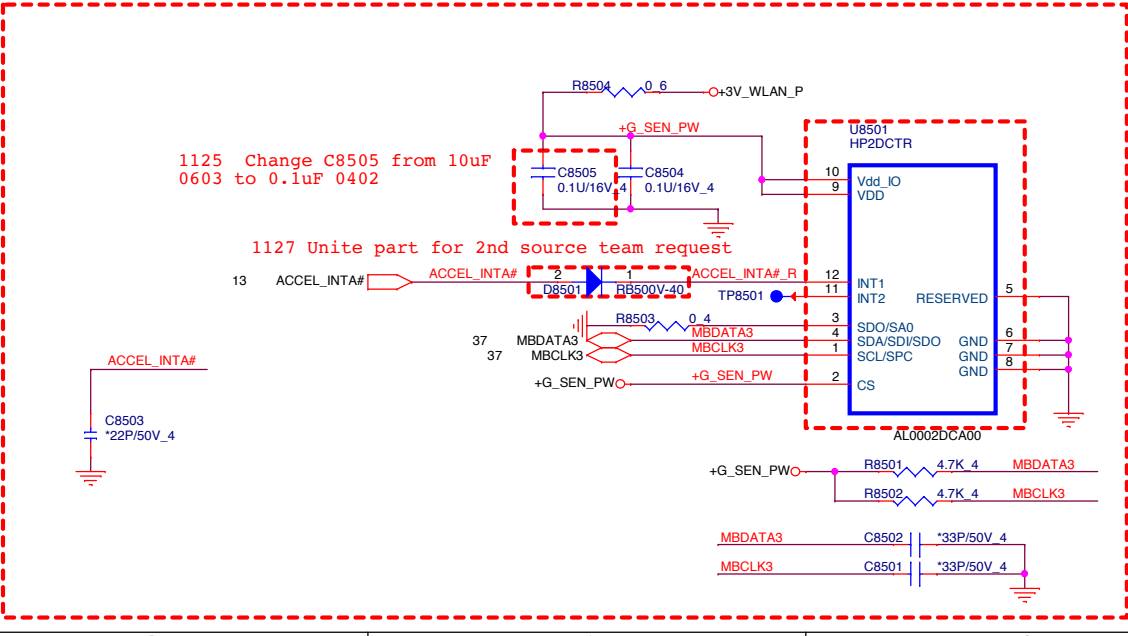
PN:AL009665K01



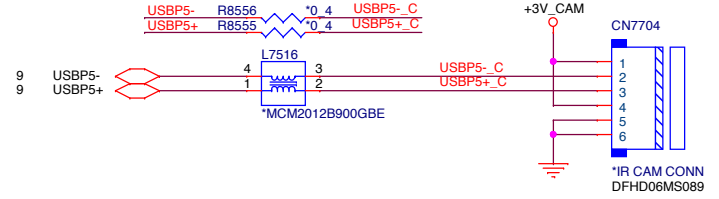
# Accelerometer Sensor

1124 Modify Accelerometer Sensor circuit follow HP2DCTR 1124.DSN

1126 Change G sensor footprint from lga12-2x2-5 to lga12-2x2-5-hp2dctr



# IR CAM



**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

Size B	Document Number 34 -- TPM/G-Sensor	Rev 1A
Date: Monday, December 28, 2015   Sheet 34 of 51		

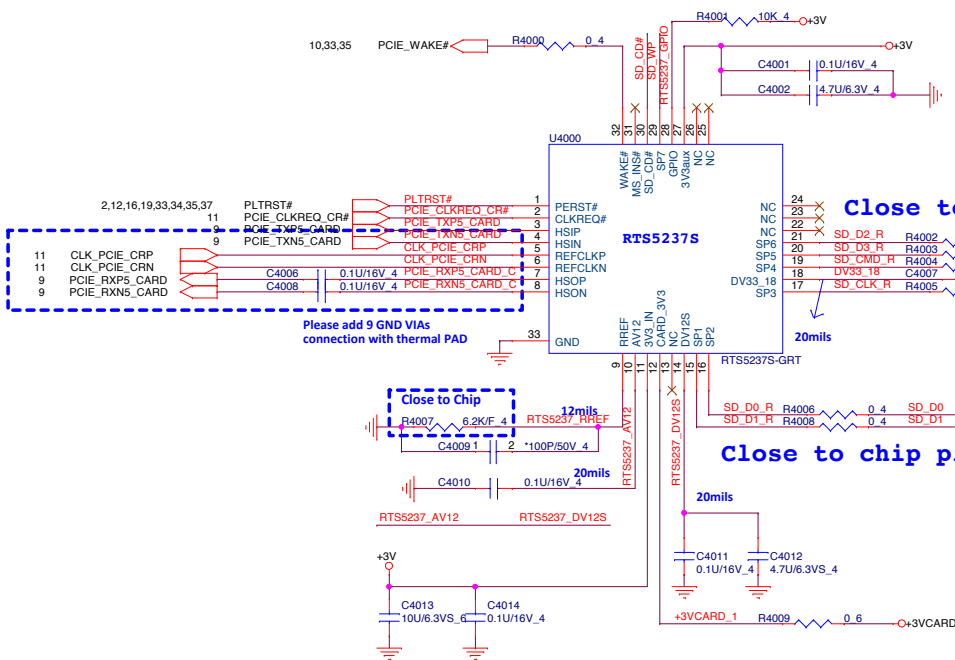


# RTS5237S PCIE CARD READER Controller

## Share Pin

SD / MMC

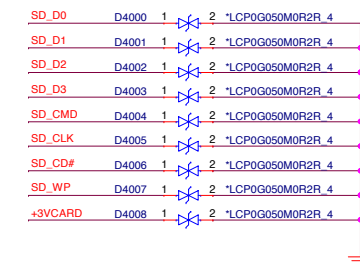
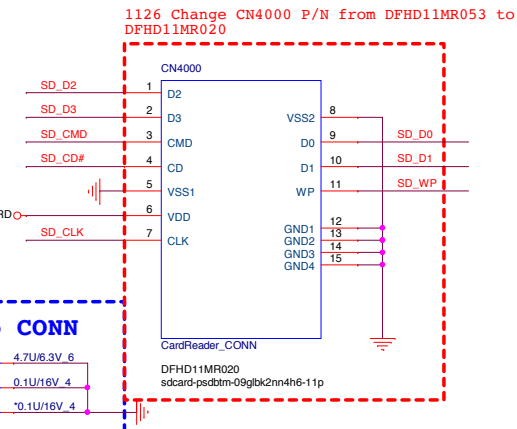
SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D0
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS



Close to chip pin

Close to chip

Close to CONN



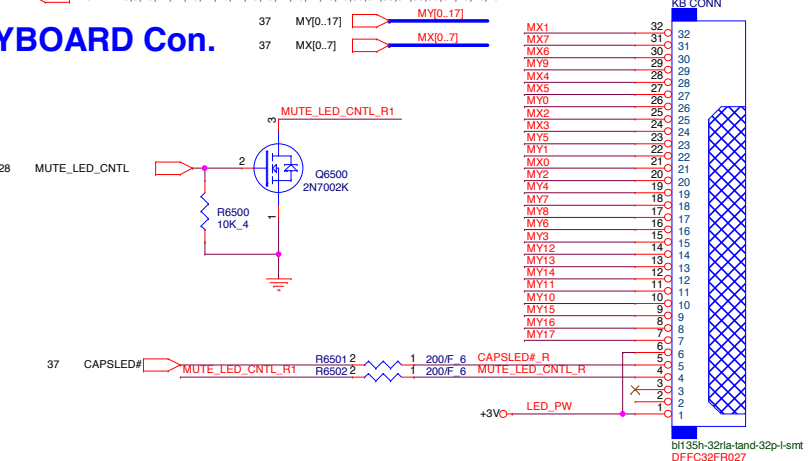
**PROJECT : G37A/G37B**  
Quanta Computer Inc.

Size Custom	Document Number <b>36 - CR RTS5237S/CR SOCKET</b>	Rev <b>1A</b>
Date: Monday, December 28, 2015   Sheet 36 of 51		

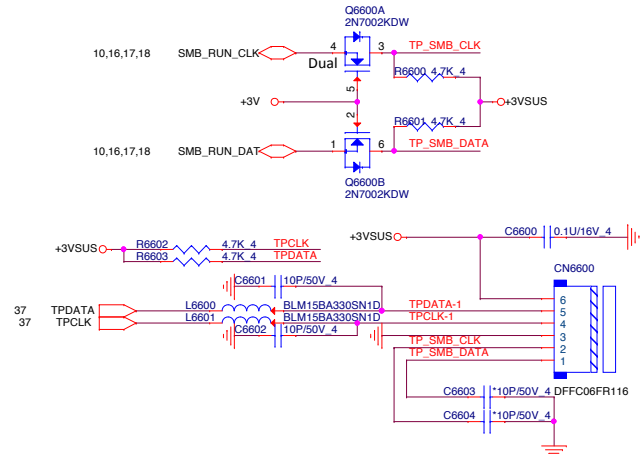


### KEYBOARD Con.

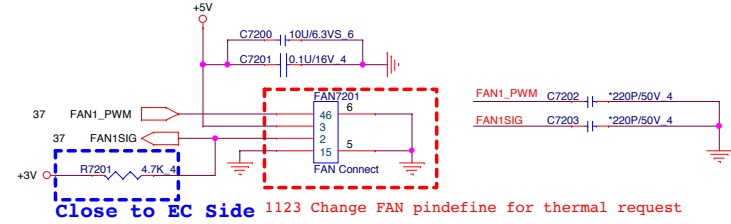
+VIN	26,32,39,40,41,42,43,44,45,47,48,49,50
+5V	26,27,28,29,31,32,46,49
+3VPCU	5,10,20,33,37,40,41
+3VSS	10,12,14,16,26,33,37,41,42,46,47,48,51
+3VSUS	46
+3V	5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,43,46,49



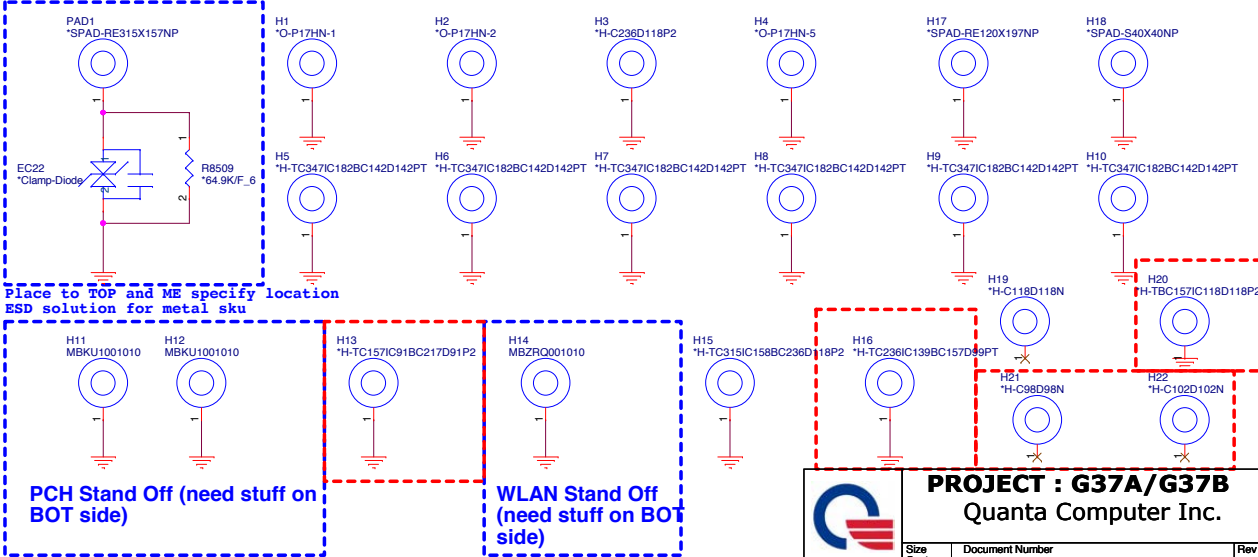
### Touch Pad Connector



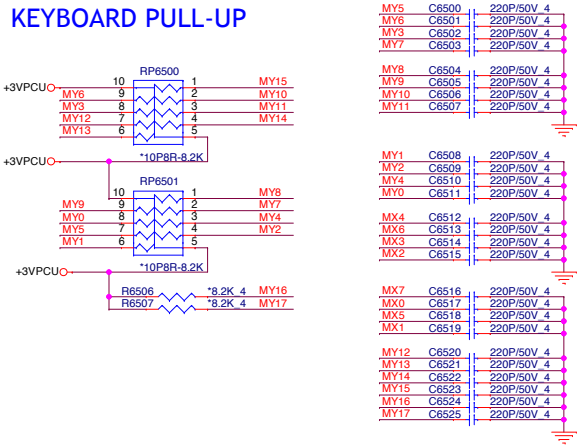
### FAN



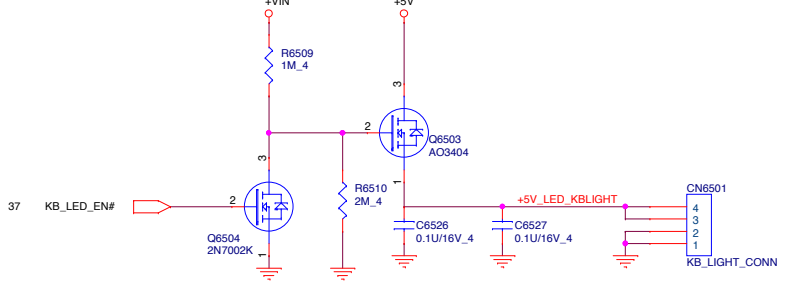
### HOLE



### KEYBOARD PULL-UP

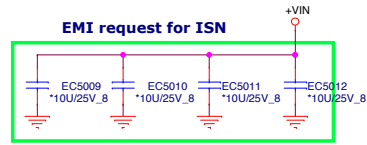
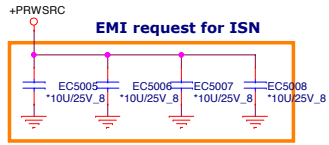



### KB LIGHT CONN

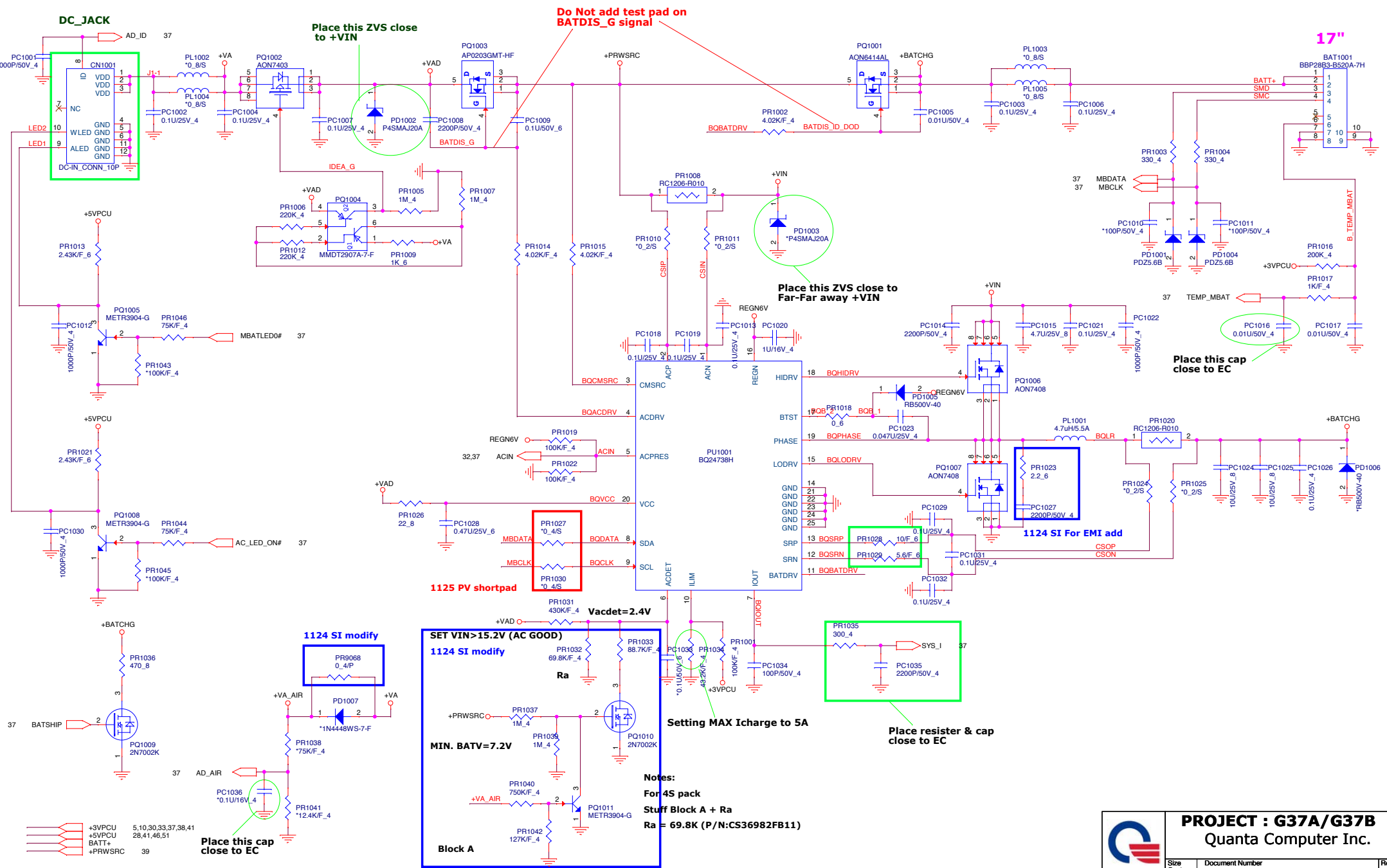



**PROJECT : G37A/G37B**  
Quanta Computer Inc.

Size Custom	Document Number 38 -- KB/KBL/TP/FAN/HOLE	Rev 1A
Date: Monday, December 28, 2015	Sheet 36 of	51

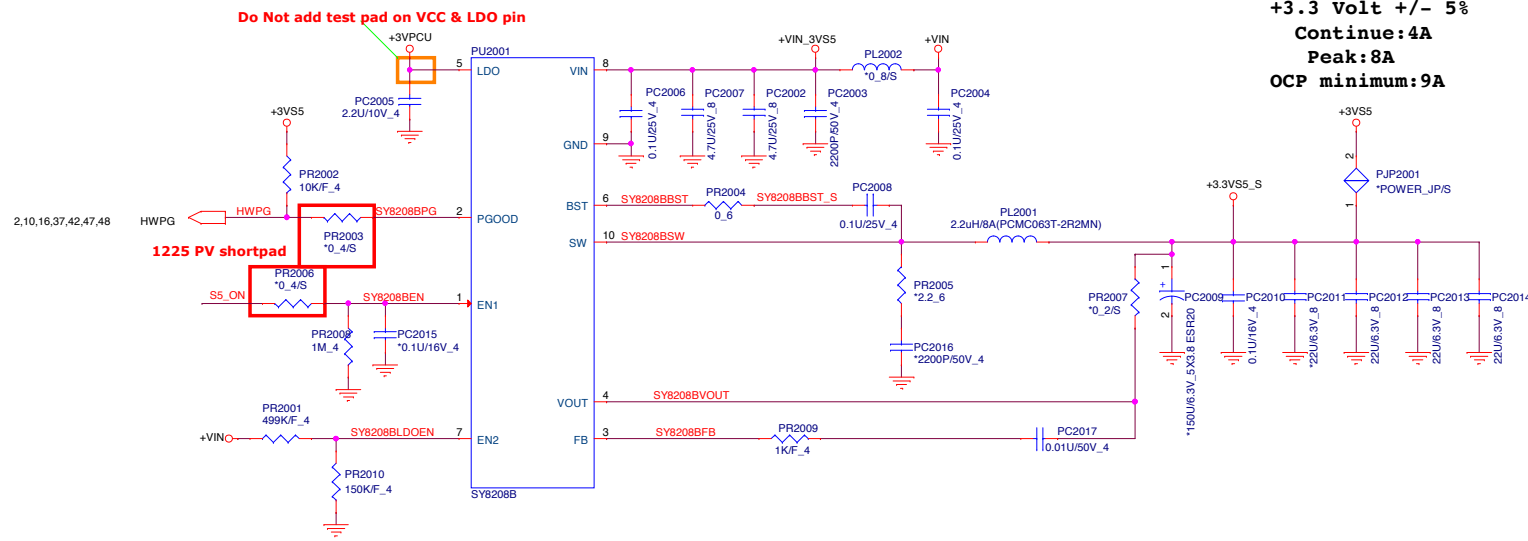


	<b>PROJECT : G37A/G37B</b>	
	Quanta Computer Inc.	
	Size Custom	Document Number <b>RF Solution</b>
Date: Monday, December 28, 2015   Sheet 39 of 51		

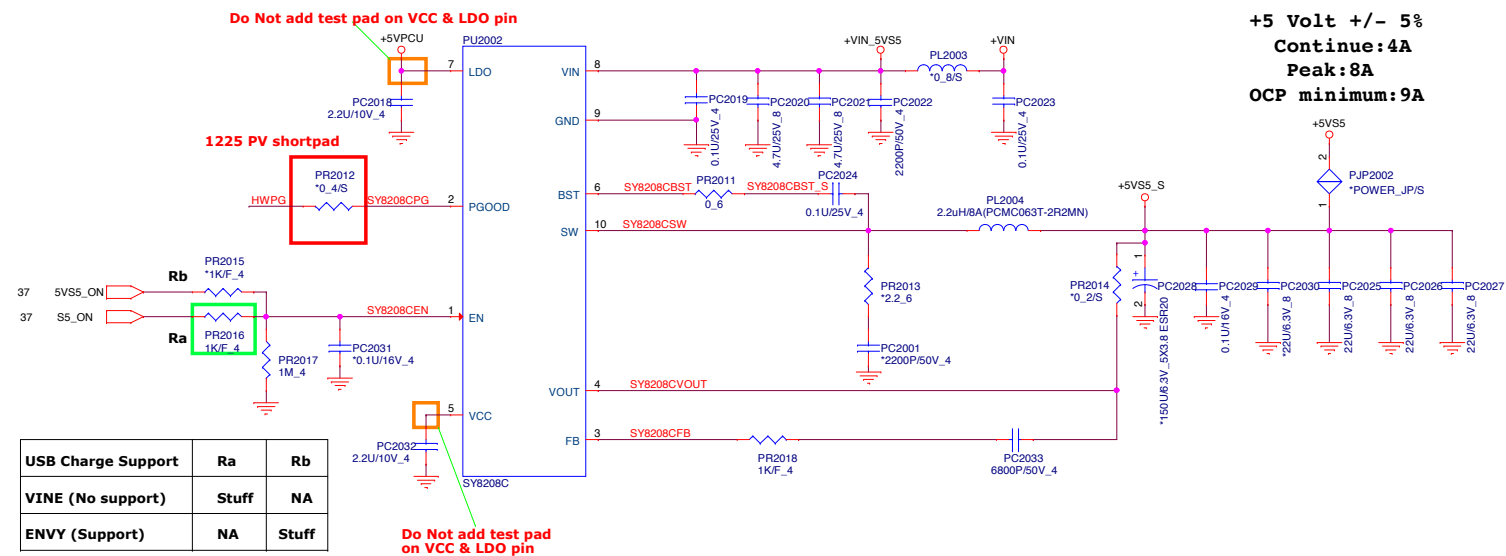


		<b>PROJECT : G37A/G37B</b>	
		Quanta Computer Inc.	
Size Custom	Document Number	Rev 1A	
		<b>Charger (BQ24738H)</b>	
Date: Monday, December 28, 2015	Sheet 40 of 51		





**+3.3 Volt +/- 5%**  
**Continue:4A**  
**Peak:8A**  
**OCp minimum:9A**



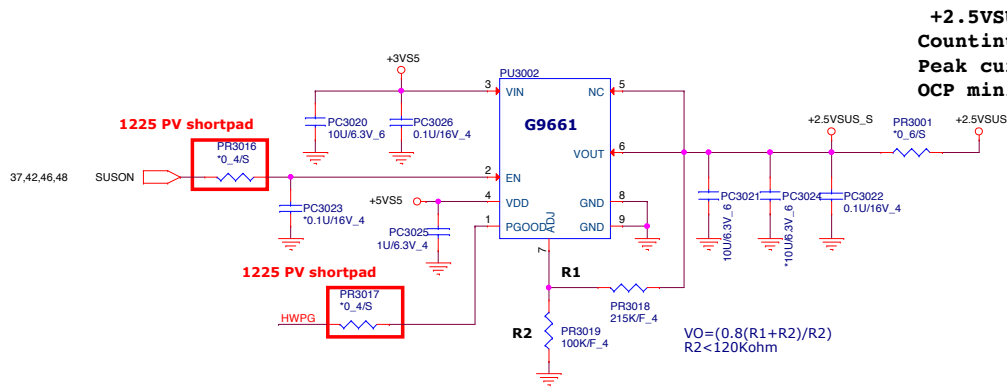
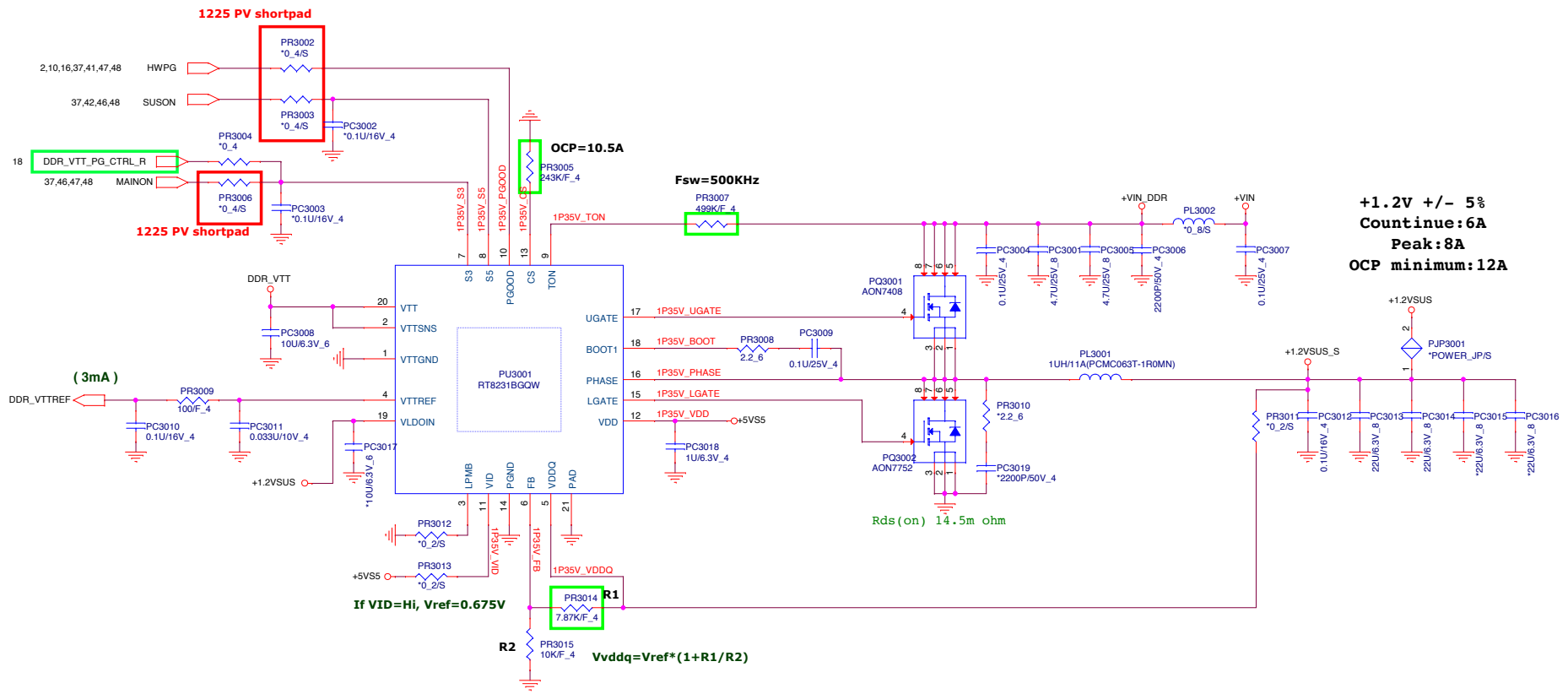
**+5 Volt +/- 5%**  
**Continue:4A**  
**Peak:8A**  
**OCp minimum:9A**

USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff


- +VIN 26,32,38,39,40,42,43,44,45,47,48,49,50
- +3VSS 10,12,14,16,26,33,37,42,46,47,48,51
- +5VSS 10,26,28,30,42,43,44,45,46,47,48,49,50,51
- +3VPCU 5,10,30,33,37,38,40
- +5VPCU 28,40,46,51

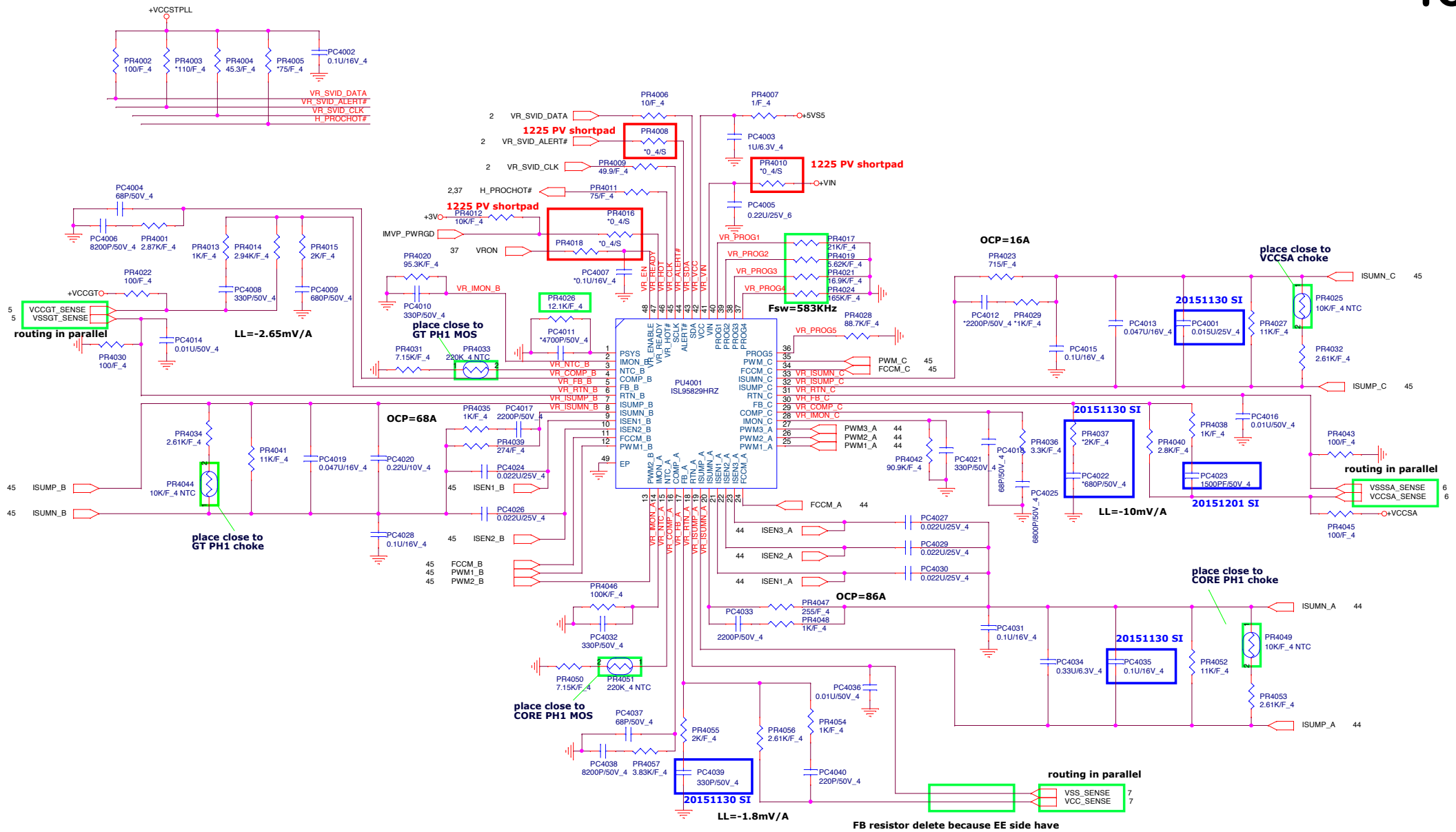
**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**


Size Custom	Document Number <b>3/5V55 (SY8208B/SY8208C)</b>	Rev 1A
Date: Monday, December 28, 2015	Sheet 41 of 51	



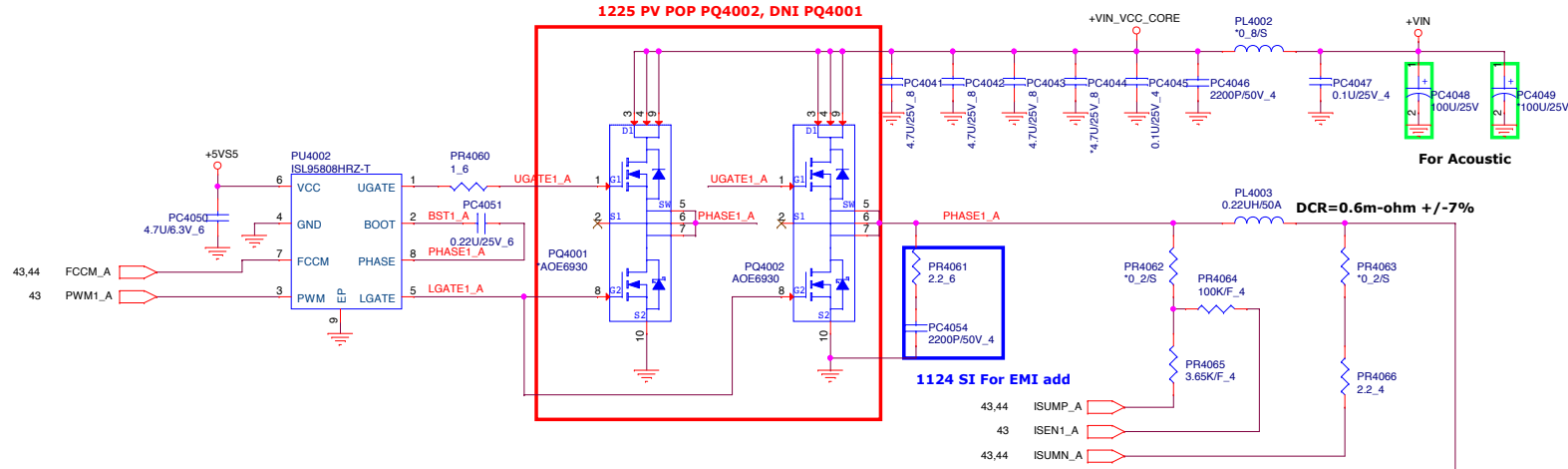
+VIN	26,32,38,39,40,41,43,44,45,47,48,49,50
+5VSS	10,26,28,30,41,43,44,45,46,47,48,49,50,51
+1.2VSUS	2,6,10,17,18,46,48,51
DDR_VTT	17,18
+2.5VSUS	17,18

 <b>PROJECT : G37A/G37B</b> <b>Quanta Computer Inc.</b>			Size
			Document Number <b>DDR3 (RT8231B)</b>
Monday, October 28, 2015		Sheet 42	of 51
			Rev 1A



 <b>PROJECT : G37A/G37B</b> Quanta Computer Inc.			Size	Document Number	Rev
			Custom	<b>CPU VR IC (ISL95829HRZ)</b>	1A
Date: Monday, December 28, 2015			Sheet	43	of 51

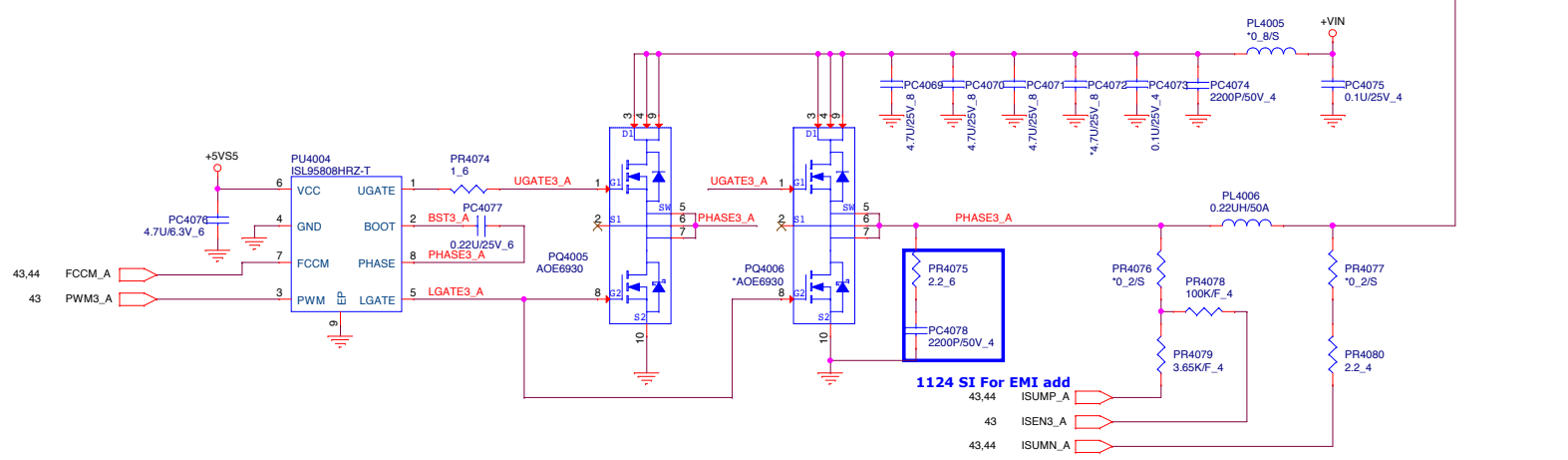
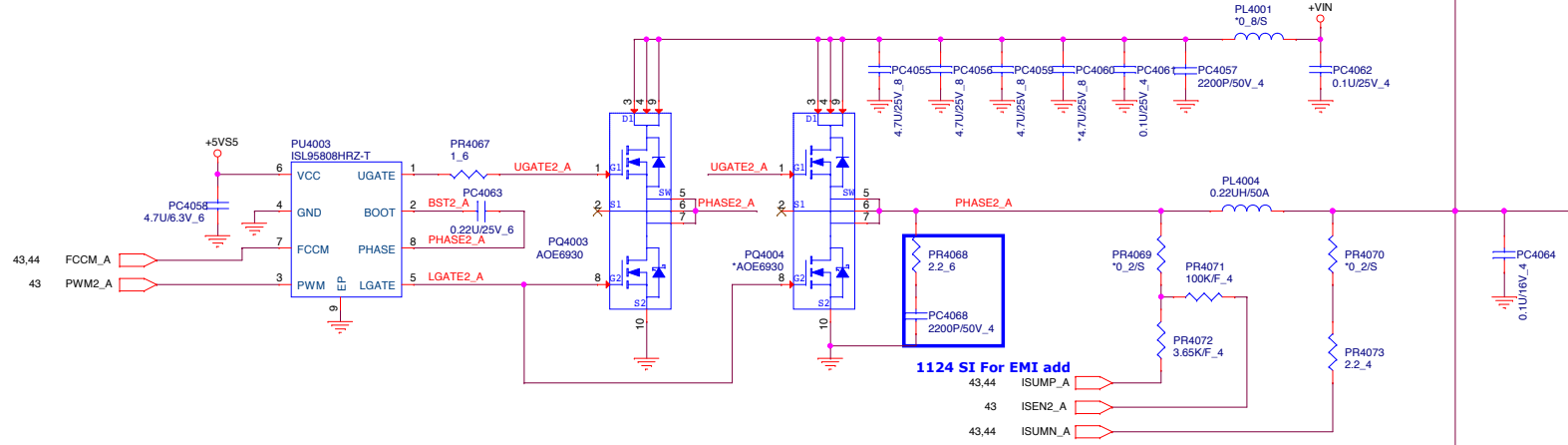
1225 PV POP PQ4002, DNI PQ4001




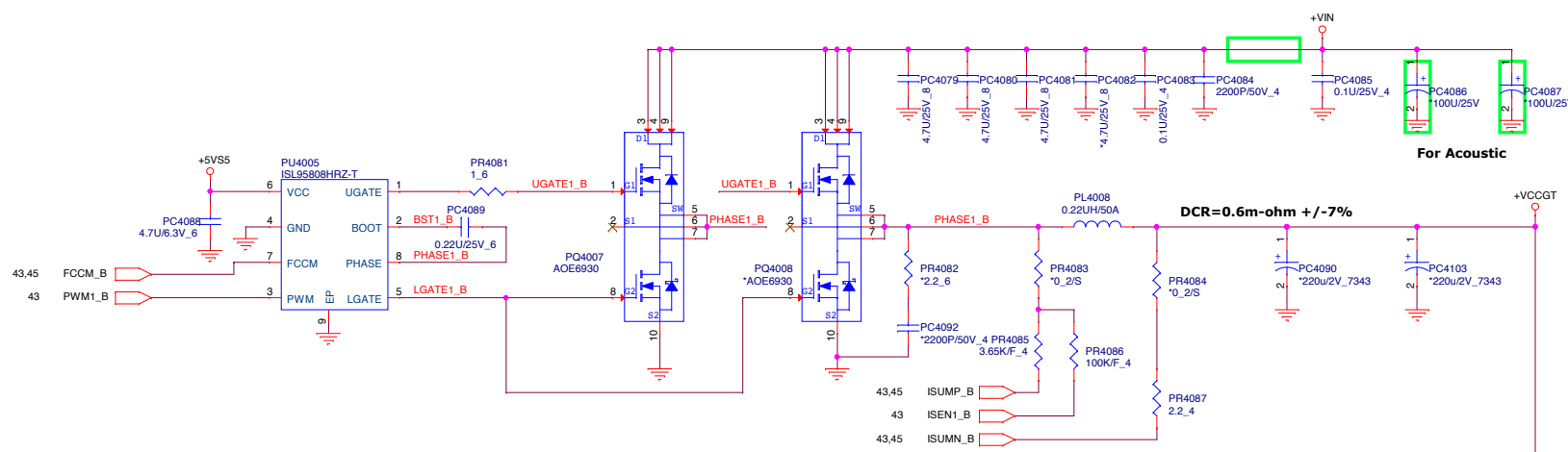
For Acoustic

**H-line42 (35W)**  
 TDC:49A  
 Iccmax:60A  
 OCP:86A  
 Loadline = -1.8 mV/A

**H-line42 (45W)**  
 TDC:56A  
 Iccmax:68A  
 OCP:86A  
 Loadline = -1.8 mV/A

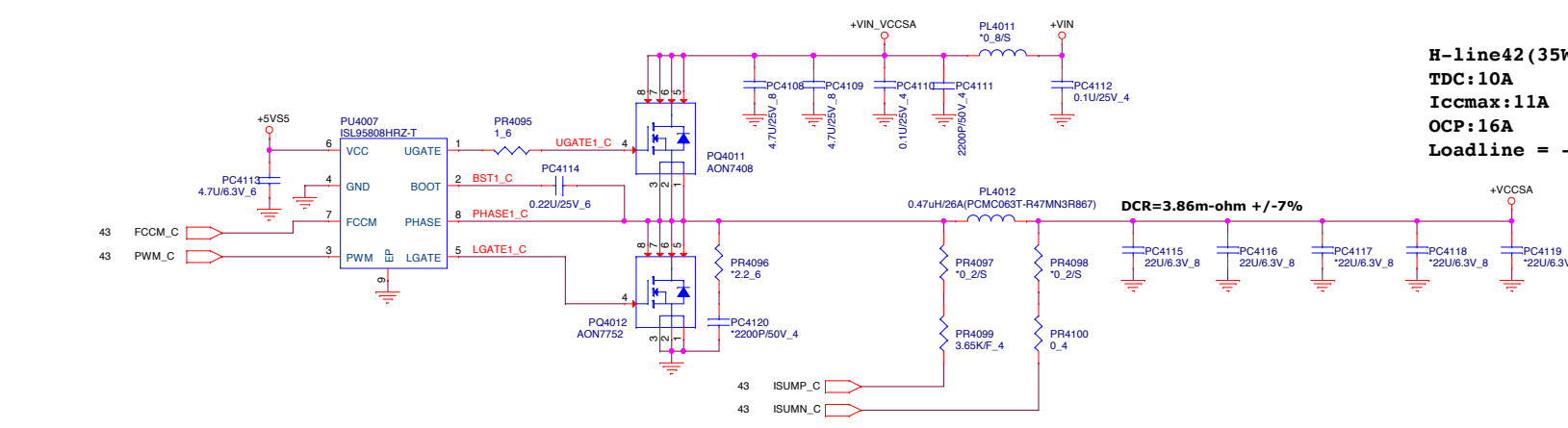
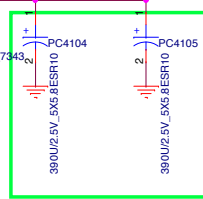
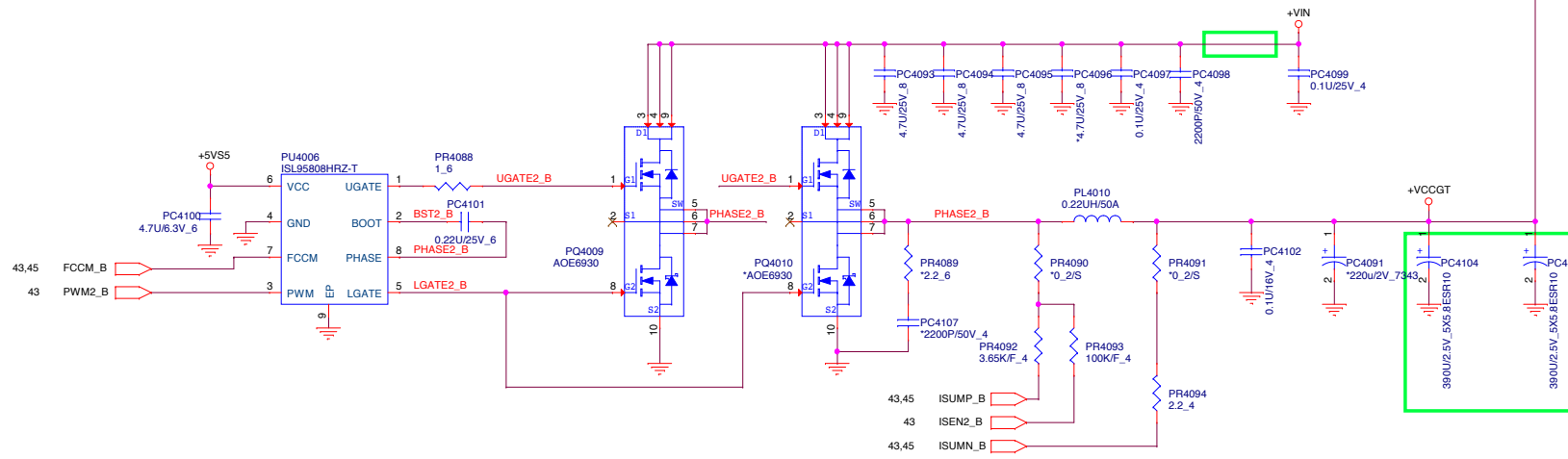


 <b>PROJECT : G37A/G37B</b> <b>Quanta Computer Inc.</b>		
Size Custom	Date: Monday, December 28, 2015   Sheet 44 of 51	



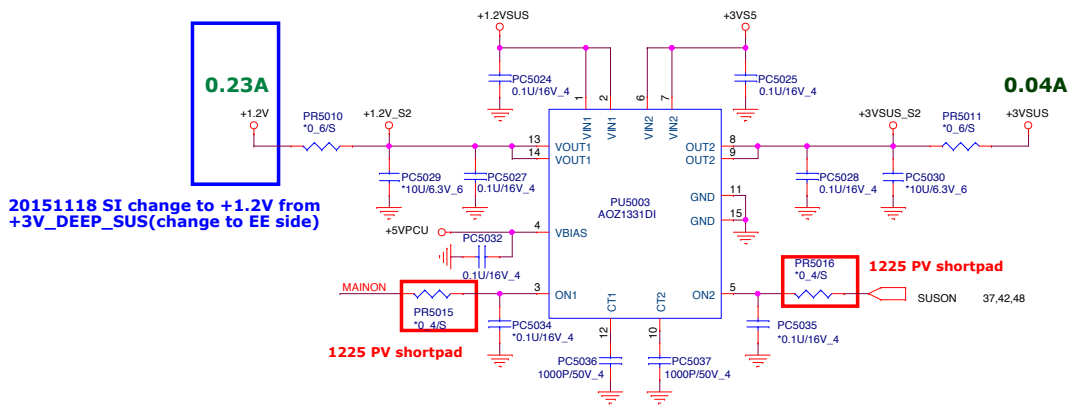
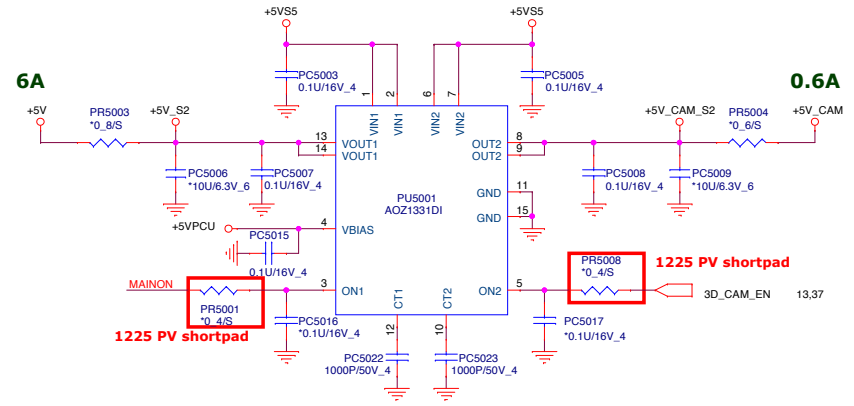
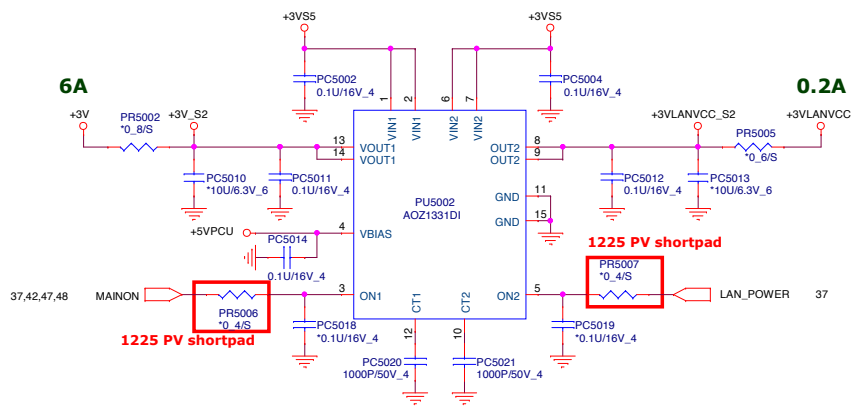
**H-line42 (35W)**  
**TDC: 41A**  
**Iccmax: 55A**  
**OCp: 68A**  
**Loadline = -2.65 mV/A**

**H-line42 (45W)**  
**TDC: 39A**  
**Iccmax: 55A**  
**OCp: 68A**  
**Loadline = -2.65 mV/A**



**H-line42 (35W/45W)**  
**TDC: 10A**  
**Iccmax: 11A**  
**OCp: 16A**  
**Loadline = -10 mV/A**


	<b>PROJECT : G37A/G37B</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number <b>+VCCGT/SA (ISL95808HRZ-T)</b>	Rev 1A
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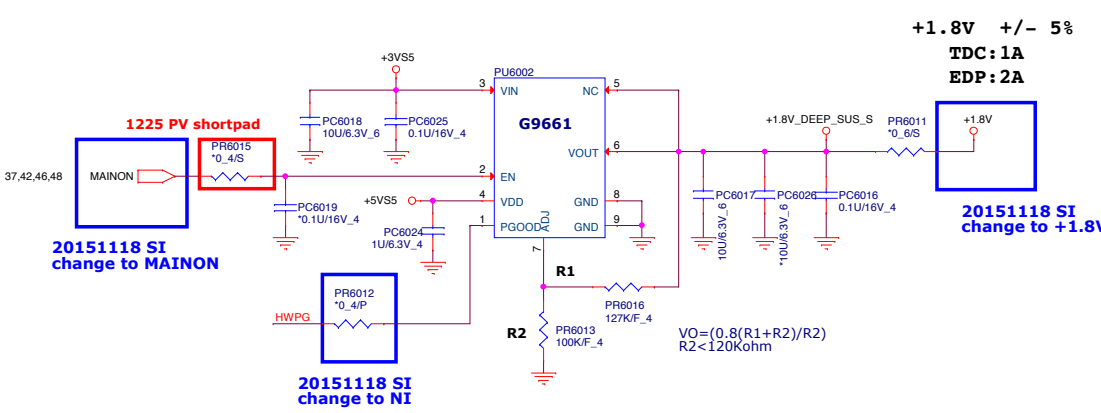
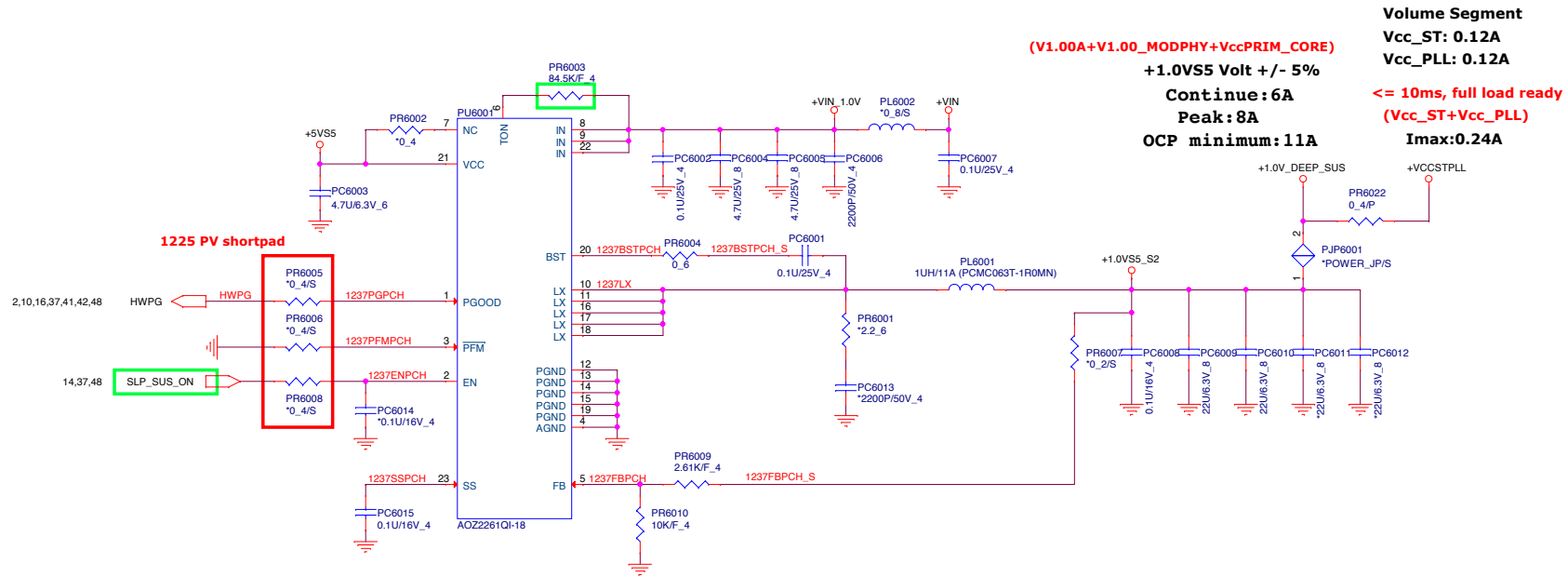


20151118 SI del +1.5V and add +1.2V



- +3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,49
- +5V 26,27,28,29,31,32,38,49
- +3VS5 10,12,14,16,26,33,37,41,42,47,48,51
- +5VS5 10,26,28,30,41,42,43,44,45,47,48,49,50,51
- +3VSUS 38
- +3VLANVCC 35
- +5V\_CAM 31
- +1.2V 27
- +3V\_DEEP\_SUS 9,10,12,13,14,16,18

		<b>PROJECT : G37A/G37B</b>	
		Quanta Computer Inc.	
Size Custom	Document Number	Rev 1A	
<b>Load switch IC (AOZ1331D)</b>			
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20151118 SI del



- +VIN 26,32,38,39,40,41,42,43,44,45,48,49,50
- +3VS5 10,12,14,16,26,33,37,41,42,46,48,51
- +5VS5 10,26,28,30,41,42,43,44,45,46,48,49,50,51
- +1.0V\_DEEP\_SUS 10,11,14,16,48
- +1.8V 28,31
- +VCCSTPLL 2,6,43



**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>+1.0_DEEP_SUS</b>	Rev 1A
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## Volume Segment

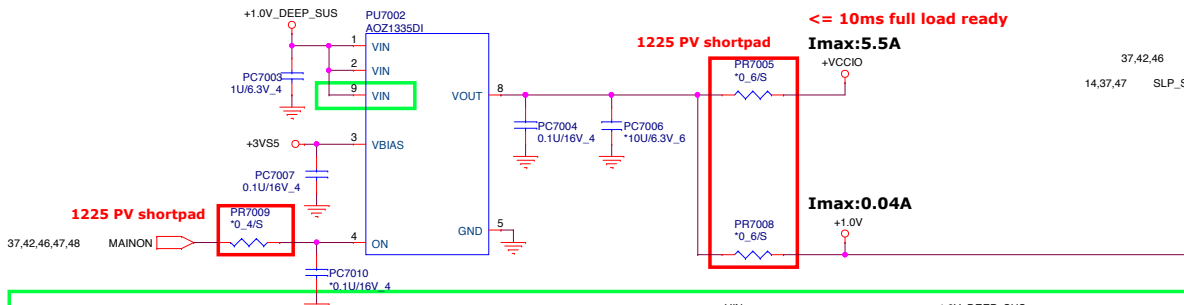
Vcc\_STG: 0.04A

Vcc\_IO: 5.5A

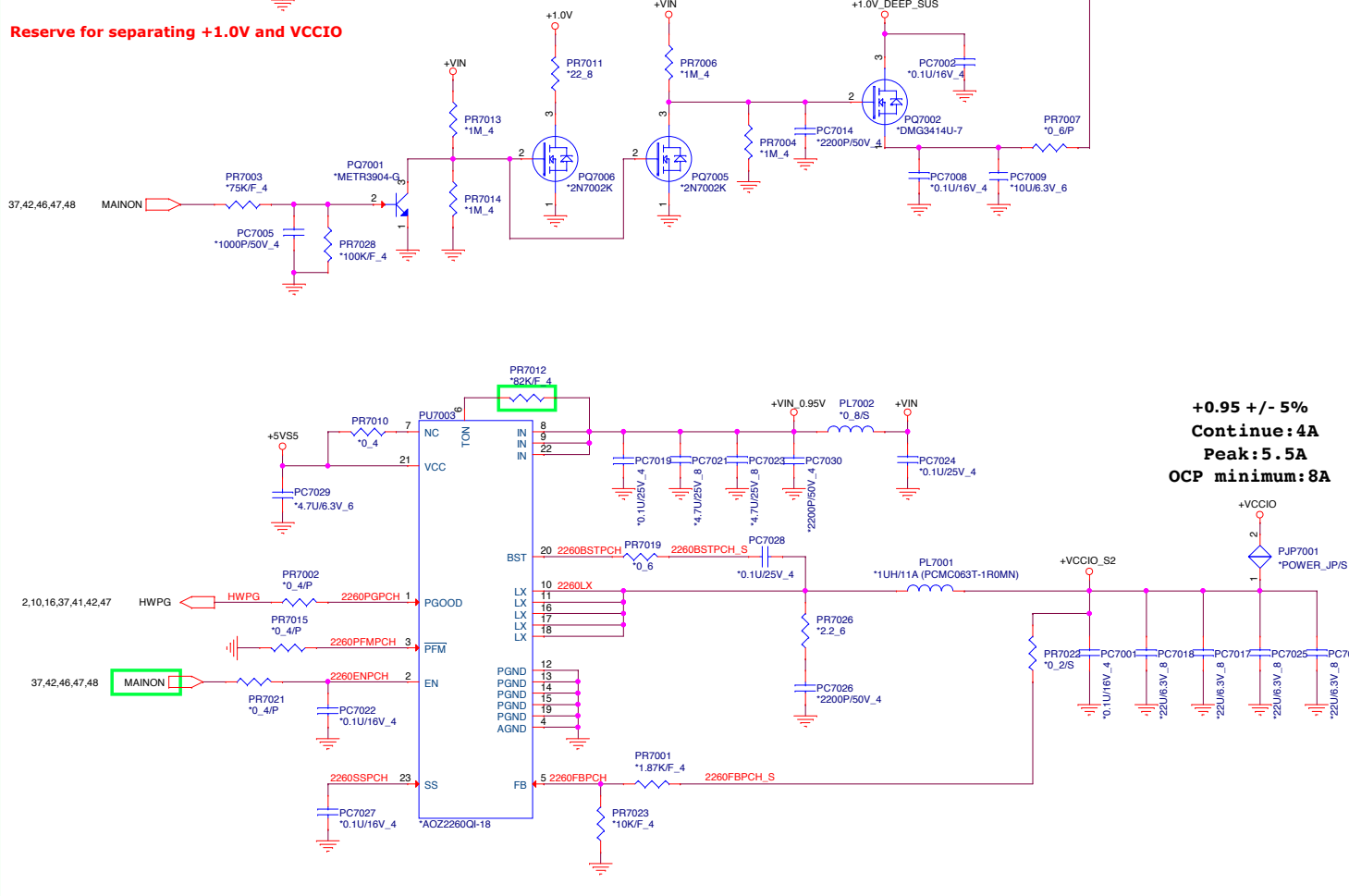
<= 10ms full load ready

Imax:5.5A

Imax:0.04A

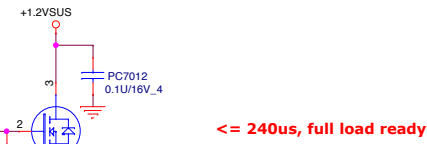
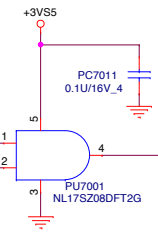
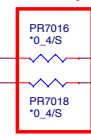


Reserve for separating +1.0V and VCCIO



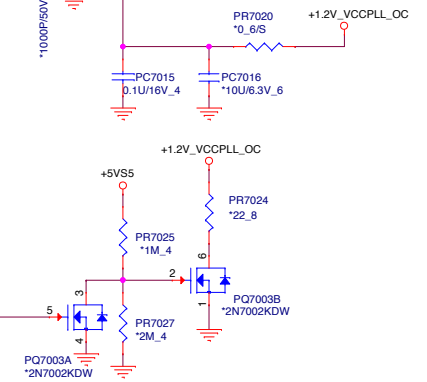
1225 PV shortpad

37,42,46 SUSEN  
14,37,47 SLP\_SUS\_ON



<= 240us, full load ready

TDC:0.26A



+0.95 +/- 5%

Continue: 4A

Peak: 5.5A

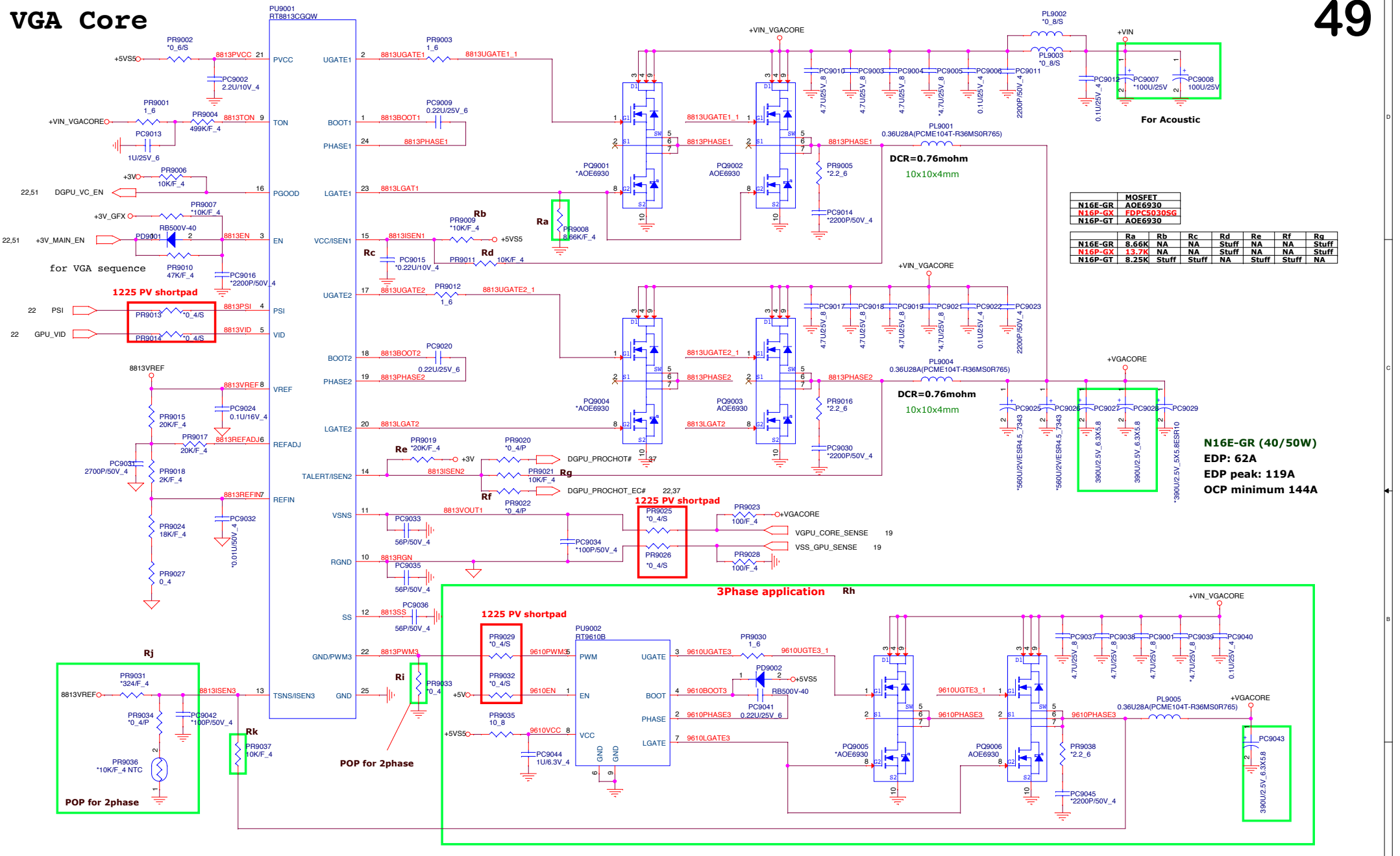
OCF minimum: 8A

+1.0V	2,5,6,10,16,37
+3V5S	10,12,14,16,26,33,37,41,42,46,47,51
+5V5S	10,26,28,30,41,42,43,44,45,46,47,49,50,51
+VCCIO	3,6,16
+1.0V_DEEP_SUS	10,11,14,16,47
+1.2V_VCCPLL_OC	6
+1.2V_SUS	2,6,10,17,18,42,46,51

**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>+1.0V/+VCCSTPLL+VCCIO</b>	Rev 1A
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	MOSFET	
N16E-GR	AOE6930	
N16P-GX	FDPC5030SG	
N16P-GT	AOE6930	

	Ra	Rb	Rc	Rd	Re	Rf	Rg
N16E-GR	8.66K	NA	NA	Stuff	NA	NA	Stuff
N16P-GX	13.7K	NA	NA	Stuff	NA	NA	Stuff
N16P-GT	8.25K	Stuff	Stuff	NA	Stuff	Stuff	NA

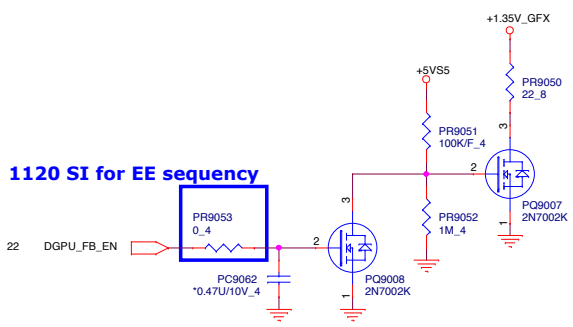
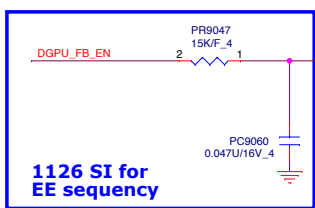
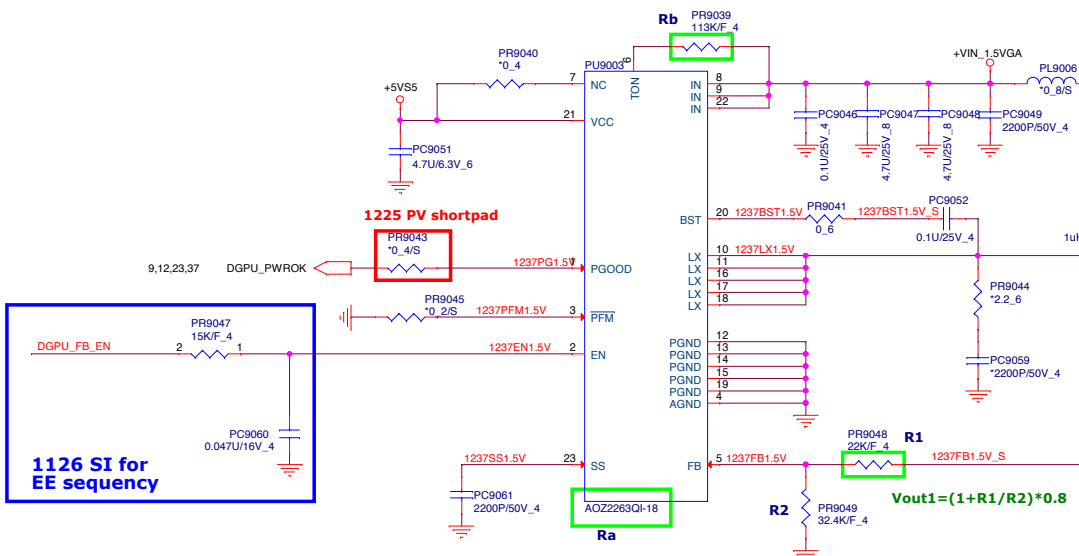
**N16E-GR (40/50W)**  
**EDP: 62A**  
**EDP peak: 119A**  
**OCV minimum 144A**

	Rh	Ri	Rj	Rk
N16E-GR	Stuff	NA	NA	Stuff
N16P-GX	Stuff	NA	NA	Stuff
N16P-GT	NA	Stuff	Stuff	NA

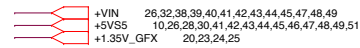
- +3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46
- +VIN 26,32,38,39,40,41,42,43,44,45,47,48,50
- +5VS5 10,26,28,30,41,42,43,44,45,46,47,48,50,51
- +3V\_GFX 19,20,21,22,23,51
- +VGACORE 23

**DDR3(1.5V / 1.35V)**  
**EDP=4.18A**  
**EDP\_peak=6.54A**  
**OCP minimum:11A**

**GDDR5(1.35V)**  
**EDP=8.9A**  
**EDP\_peak=11.9A**  
**OCP minimum:13A**



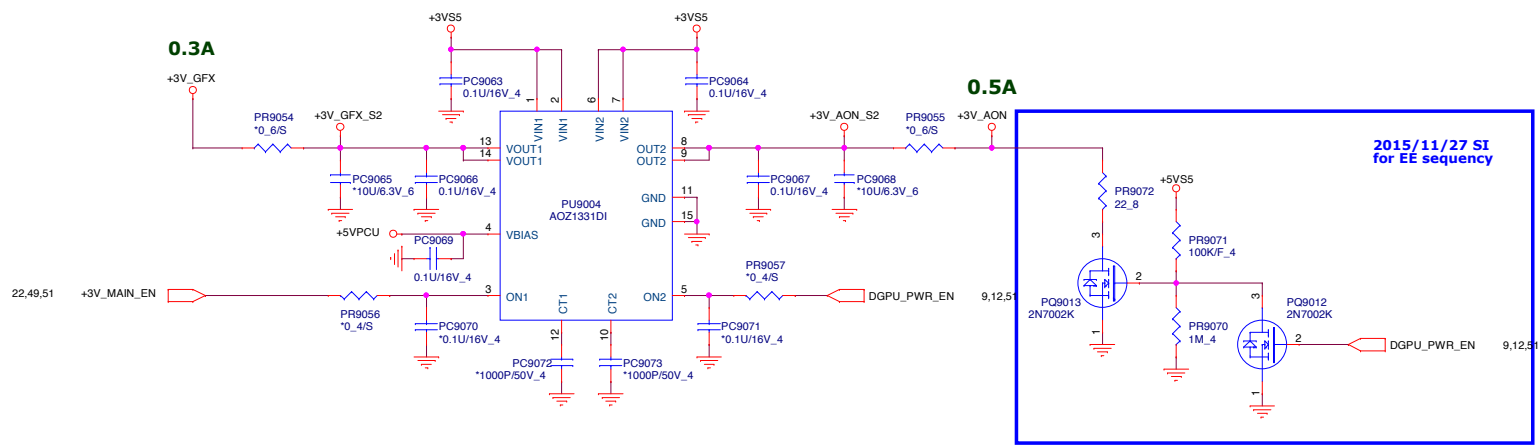
	Ra	Rb	R1
<b>DDR3 (1.5V)</b>	<b>AOZ2261QI-18</b>	<b>127K</b>	<b>28.7K</b>
<b>DDR3 (1.35V)</b>	<b>AOZ2261QI-18</b>	<b>113K</b>	<b>22K</b>
<b>GDDR5(1.35V)</b>	<b>AOZ2263QI-18</b>	<b>113K</b>	<b>22K</b>



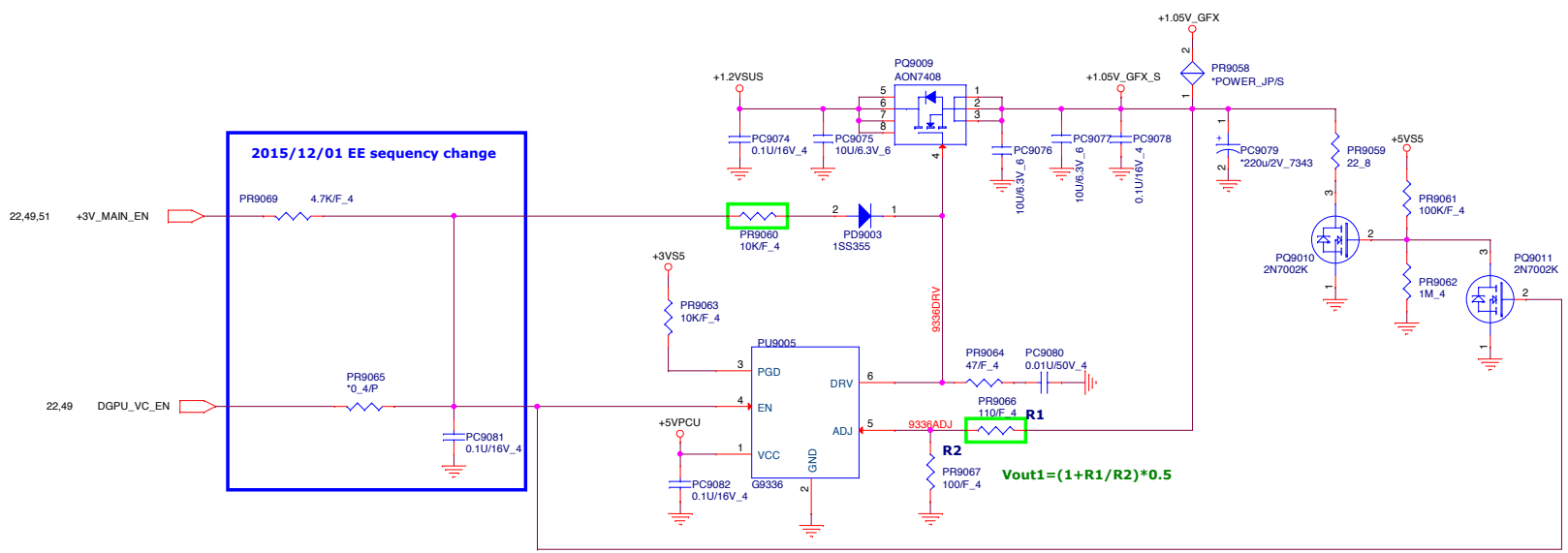
**PROJECT : G37A/G37B**

**Quanta Computer Inc.**


Size Custom	Document Number <b>+1.35V_GFX (AOZ2263QI-18)</b>	Rev 1A
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**+1.05V\_GFX Volt +/- 5%**  
**EDP=2.38A**  
**EDP\_peak = 2.45A**



- +VIN 26,32,38,39,40,41,42,43,44,45,47,48,49,50
- +3VS5 10,12,14,16,26,33,37,41,42,46,47,48
- +5VS5 10,26,28,30,41,42,43,44,45,46,47,48,49,50
- +3V\_GFX 19,20,21,22,23,49
- +3V\_AON 19,22,23,27
- +1.2VSUS 2,6,10,17,18,42,46,48
- +1.05V\_GFX 19,20,21,23

 <b>PROJECT : G37A/G37B</b> Quanta Computer Inc.		